Design and Implementation of High Conversion Efficiency RF to DC Rectifier Based on Inverted Gate Topology of Class F GaN HEMT RF High Power Amplifier for Wireless Power Transfer

Final Project

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2026

STATEMENT OF AUTHENTICITY OF FINAL PROJECT

I, the undersigned, certify that the contents of part or all of my Final Project entitled: "Design and Implementation of High Conversion Efficiency RF to DC Rectifier Based on Inverted Gate Topology of Class F GaN HEMT RF High Power Amplifier For Wireless Power Transfer" is my own work, completed without the use of materials that are not permitted, and is not the work of other parties which I acknowledge as my own work. All references cited or referred to have been written in full in the bibliography. If it turns out that my statement is not true, I am willing to accept sanctions in accordance with applicable regulations.

Batam, 24th July 2026

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Design and Implementation High Efficiency RF to DC Rectifier Based on Inverted Gate Topology of Class F GaN HEMT RF High Power Amplifier

ABSTRACT

This final project presents the design of a high-efficiency RF-to-DC rectifier based on the inverted gate topology of a Class-F GaN HEMT RF high power amplifier for wireless battery charging applications. The proposed rectifier utilizes the time-reversal duality principle to convert RF energy into DC power efficiently. The circuit employs a CGH40010F GaN HEMT transistor operating at 2.6 GHz and is implemented on a Rogers RO4350B substrate with a dielectric constant of 3.66. The design consists of an input matching network, harmonic termination network, gate and drain bias networks, and an RF-to-DC output filtering circuit to maximize power conversion performance. The proposed rectifier was analyzed through circuit simulation using Keysight Advanced Design System (ADS) by varying the RF input power while maintaining a constant operating frequency of 2.6 GHz. Simulation results show that the rectifier achieves a maximum RF-to-DC power conversion efficiency of 66.487% with a DC output power of 8.415 W at an input power of 40 dBm. These results demonstrate that the proposed inverted gate topology effectively improves RF-to-DC energy conversion and has strong potential for high-power wireless power transfer (WPT) and rectenna-based wireless battery charging applications.

*Keywords**: RF-to-DC Rectifier, GaN HEMT, Inverted Gate Topology, Class-F Power Amplifier, Wireless Power Transfer, Rectenna.***

FOREWORD

The author expresses gratitude to Almighty God for His mercy and guidance, enabling the author to successfully complete this final project entitled "Design and Implementation Rectifying of Inverted Power Amplifier for Rectenna of Wireless Battery Charging." The writing of this final project is one of the academic requirements for completing the Manufacturing Electronics Engineering study program at Batam State Polytechnic.
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Design and Implementation High Efficiency RF to DC Rectifier Based on Inverted Gate Topology of Class F GaN HEMT RF High Power Amplifier

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***Abstract*— This research presents the design and implementation of a high conversion efficiency RF-to-DC rectifier based on the inverted gate topology of a Class-F GaN HEMT RF high-power amplifier for wireless power transfer applications. Efficient electromagnetic power conversion is critical for wireless energy harvesting and battery charging systems to deliver reliable power without direct physical contact. The main component developed in this study utilizes the CGH40010F GaN HEMT transistor, applying time-reversal duality principles to convert RF power into DC energy at an operating frequency of 2.6 GHz. Based on this approach, the research is conducted under the title "Design and Implementation of High Conversion Efficiency RF to DC Rectifier Based on Inverted Gate Topology of Class F GaN HEMT RF High Power Amplifier". The proposed rectifier was implemented on a Rogers 4350 substrate by combining a coupler and a phase shifter to achieve the desired harmonic impedance termination. Harmonic Balance (HB) simulation results demonstrate robust performance, achieving a DC output voltage of 18.23 V, a DC output current of 0.385 A, and a power conversion efficiency (PCE) of 66.89% at an input power of 40 dBm. Despite minor efficiency degradation caused by substrate dielectric losses and layout parasitic effects at harmonic frequencies, this study successfully demonstrates the high-power capability and efficiency of GaN-based inverted Class-F rectifiers for advanced wireless power systems.**

Keywords: Coupler, DC power, Efficiency, Phase Shifter, Wireless charging

I. INTRODUCTION

Wireless technology continues to advance, the demand for wireless charging systems is growing rapidly. One of the key technologies enabling wireless charging is Wireless Power Transfer (WPT), which allows devices to charge without physical connectors or cables [1]. This technology is highly sought after across various sectors, from consumer electronics to electric vehicles (EV). In areas with limited electrical infrastructure, operational time constraints, and minimal human resources, wireless charging technology is essential because it enables automated charging without direct contact with a physical charging station, thereby eliminating manual operation and significantly reducing downtime during charging [2].

Wireless Power Transfer (WPT) technology can be broadly categorized into two fundamental classifications: near-field and far-field systems. Near-field WPT systems utilize non-radiative energy interaction mechanisms at limited operating distances within near-field electromagnetic environments [3]. Near-field approaches are generally classified into three types:

a) Capacitive Coupling:
Uses electrostatic fields to transfer electrical energy, enabling penetration through metallic barriers without significant disruption.

b) Inductive Coupling:
Operates on the principle of electromagnetic induction, where a varying current in the primary coil induces a potential difference across the secondary coil.

c) Magnetic Resonant Coupling:
Occurs when transmitter and receiver coils are tuned to identical resonant frequencies, enabling efficient energy transfer through synchronized magnetic fields.

Conversely, far-field WPT systems operate on the transmission and reception of radiated electromagnetic waves over relatively long distances using transmitter and receiver antennas [3]. A far-field WPT system begins with a power source converted into radio frequency (RF) energy, amplified through a power amplifier, and radiated through the air medium. At the receiving end, an antenna captures the incoming RF signal and passes it to a rectifier circuit to convert the captured electromagnetic waves back into usable DC electrical energy [4].

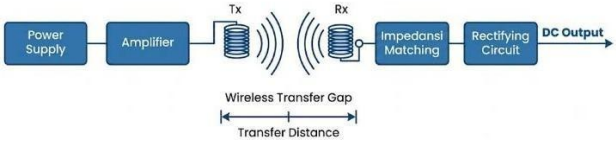


Figure 1. Topology of a Far Field Wireless Power Transfer System.

The critical challenge in far-field WPT systems lies in converting electromagnetic waves into usable DC power efficiently [5]. Applying

the principle of time-reversal duality, a high-efficiency RF power amplifier architecture can be inverted into an efficient RF-to-DC rectifier system [5]. Among high-efficiency topologies, Class-F and inverse Class-F architectures are particularly attractive because they utilize harmonic impedance manipulation—shaping fundamental and harmonic frequency terminations—to minimize power dissipation and maximize conversion efficiency [9].

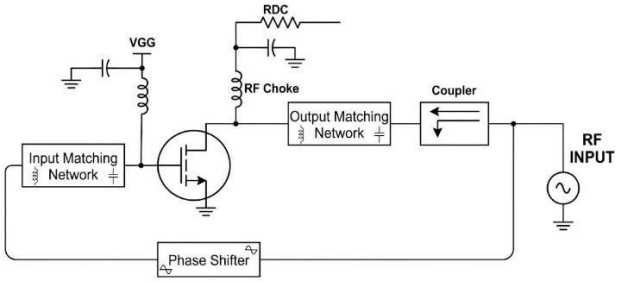


Figure 2. Topology of an Inverted Power Amplifier-Based RF-to-DC Rectifier.

To implement an inverted Class-F RF power converter operating at high frequencies and high power levels, the selection of appropriate semiconductor devices is paramount. Field Effect Transistors (FETs) regulate current flow through voltage control at the gate terminal [6, 7]. For high-power RF applications in WPT systems, Gallium Nitride High Electron Mobility Transistors (GaN HEMTs), such as the CGH40010F, offer superior characteristics over conventional transistors like silicon (Si). Due to their higher electron mobility, higher threshold voltage, and lower power loss, GaN HEMTs enable operation at higher power levels with significantly improved power efficiency and high-frequency capabilities [8].

On the other hand, impedance matching between the power amplifier, antenna, and rectifier is also a crucial factor affecting overall power transfer efficiency [9]. If the impedances are not properly matched, a substantial portion of the transmitted power can be reflected back to the source, degrading overall system performance. In an inverted gate topology of a Class-F GaN HEMT rectifier, integrating a coupler and a phase shifter allows precise adjustment of signal phase and harmonic impedance termination [10]. When fabricated on a low-loss Rogers 4350 microstrip substrate at an operating frequency of 2.6 GHz, this configuration provides optimal power handling and high conversion efficiency.

This paper presents the design and implementation of a high conversion efficiency RF-to-DC rectifier based on the inverted gate topology of a Class-F GaN HEMT RF high-power amplifier. By leveraging the CGH40010F GaN HEMT and time-reversal duality principles at 2.6 GHz, the proposed design optimizes harmonic termination to maximize DC power extraction for wireless battery charging applications.

II. DESIGN METHODOLOGY AND IMPLEMENTATION

A. Methodology

This research applies a comprehensive methodological approach by combining experimental design and simulation techniques to realize a high-efficiency RF-to-DC converter for wireless power transfer applications. The methodology integrates fundamental theoretical analysis to master the principles of reverse (inverted) Class-F RF power amplifiers—which convert RF energy into DC power—with applied research for circuit design and experimental verification of the hardware performance.

The initial stage begins with a comprehensive literature review on inverted Class-F RF power amplifiers, harmonic termination strategies, and wireless battery charging systems. The next phase involves designing and modeling the RF-to-DC power converter using Advanced Design System (ADS) simulation software. In this inverted Class-F topology operating at 2.6 GHz, the CGH40010F Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) from MACOM is selected as the primary active device due to its high breakdown voltage, superior electron mobility, and high-frequency power handling capabilities.

To design an inverted Class-F RF-to-DC power converter, several sequential design stages are executed in ADS. The complete design procedure is illustrated in the flowchart below.

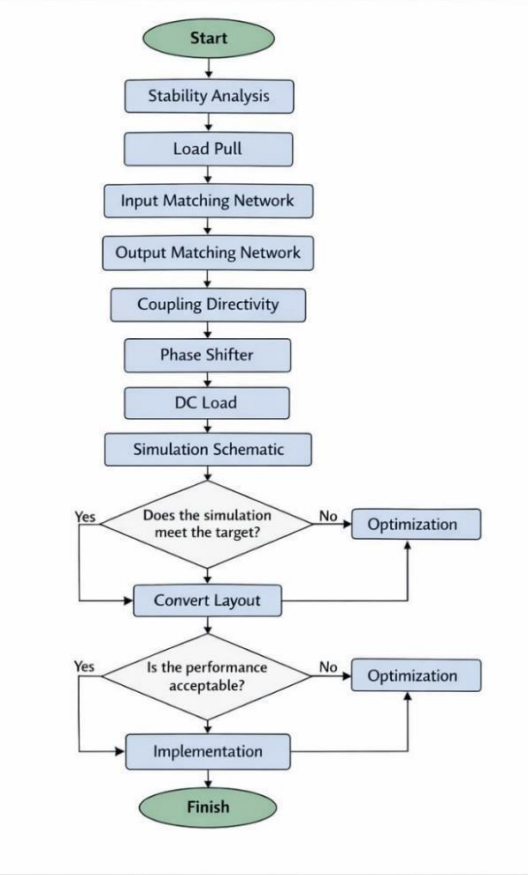


Figure 3. Flowchart Retifier Design

a. Stability Analysis

The first step in designing a GaN HEMT-based rectifier circuit is to evaluate the stability of the active device to ensure it remains free from unwanted parasitic oscillations across the operating frequency range. A transistor is defined as unconditionally stable if the Rollett stability factor $k > 1$ and the stability measure $|\Delta| < 1$, where Δ is defined as:

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

The stability factor k is expressed as:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

The stability evaluation setup and schematic in ADS for the CGH40010F transistor are depicted below.

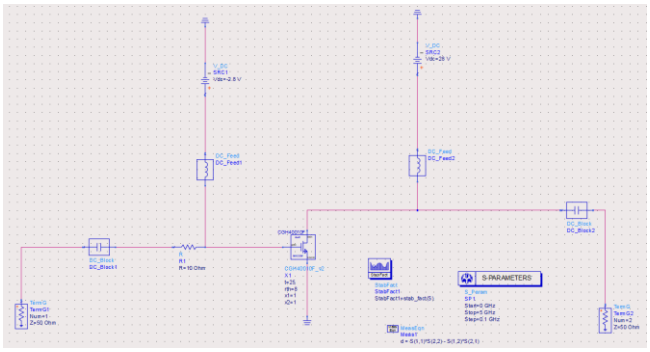


Figure 4 . Design Schematic Stability analysis

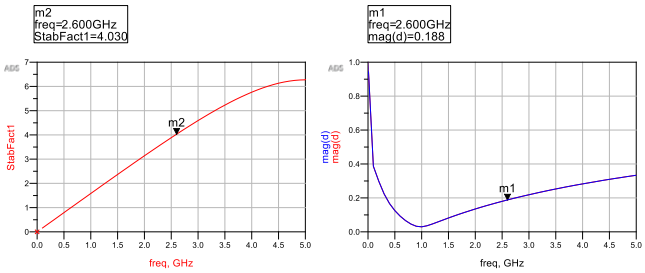


Figure 5 . Simulation result design stability analysis

The simulation results in Figure 5 confirm that the transistor is unconditionally stable across the operating frequency range. As shown in the graphs, the stability factor stays above 1 ($k > 1$) and Delta remains below 1 ($|\Delta| < 1$). These two conditions ensure that the transistor will not experience unwanted self-oscillations at any load impedance. Additionally, parameters such as Maximum Available Gain (MAG) and Maximum Stable Gain (MSG) further confirm that the circuit is completely stable, making it safe to proceed to the impedance matching stage.

b. Load pull

Load-pull A Load-Pull simulation is conducted to identify the optimal load and source impedance values (Z_{load} and Z_{source}) required to achieve maximum power conversion performance at 2.6 GHz. Unlike standard power amplifiers—where Load-Pull aims to maximize Power Added Efficiency (PAE) and output power—Load-Pull in an inverted Class-F RF-to-DC rectifier focuses on determining impedance contours that maximize DC power output (P_{DC}) and Power Conversion Efficiency (PCE) while minimizing internal reflection losses.

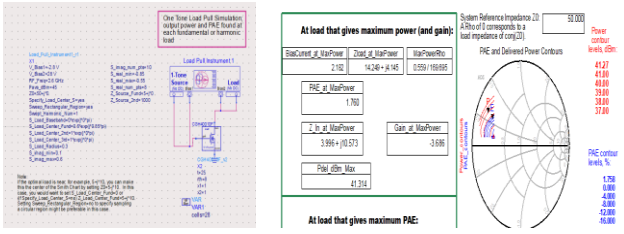


Figure 6. Design and simulation of load pull

Figure 6 illustrates the Load-Pull simulation schematic using the CGH40010F GaN HEMT. The gate bias voltage is set to $V_{GG} = -2.7$ V and the drain bias supply is set to $V_{DD} = 28$ V. The Load-Pull analysis was evaluated over an input power (P_{in}) sweep ranging from 24 dBm to 41 dBm to determine the ideal fundamental and harmonic impedance points for high-efficiency operation.

Pin	VDC	IDC	PDC	Efficiency	PAE1
33.000	7.627	0.153	1.163	58.730	21.584
34.000	8.641	0.173	1.493	59.748	20.849
35.000	9.804	0.196	1.922	60.971	20.065
36.000	11.130	0.223	2.478	62.340	19.268
37.000	12.631	0.253	3.191	63.712	18.517
38.000	14.309	0.286	4.095	64.928	17.861
39.000	16.170	0.323	5.229	65.857	17.332
40.000	18.228	0.365	6.645	66.487	16.919
41.000	20.512	0.410	8.415	66.892	16.599

Table 1. RF-To-DC Conversion Performance Under Input Power Sweep

The following is a graph of the RF input sweep simulation results from 33 dBm to 41 dBm.

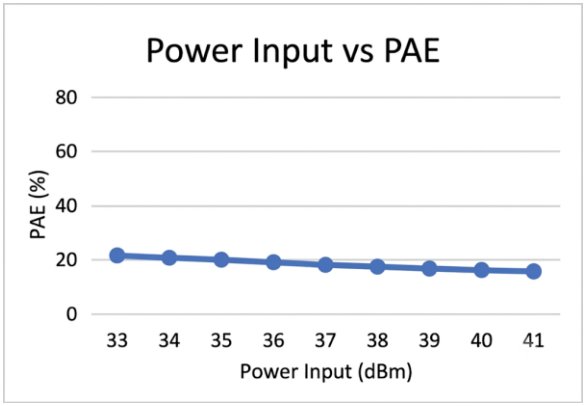


Figure 7. Power Input vs PAE graph in loadpull simulation

The figure above shows the relationship between input power (P_{in}) (dBm), Power Added Efficiency (PAE) (%), and conversion efficiency in an inverted rectifier. From the graph, it can be seen that PAE starts at around 21.6% at an input power of 33 dBm, then decreases gradually until it reaches its lowest point at around 16.6% at an input power of 41 dBm. Conversely, the power conversion efficiency to DC consistently increases from 58.7% until reaching its peak at approximately 66.9% at an input power of 41 dBm.
The characteristics of this curve show that there is an optimal operating point at an input power of around 41 dBm, where the system operates at maximum RF-to-DC conversion efficiency. The pattern of PAE decline as input power increases illustrates the component saturation phenomenon commonly observed, where at high power levels the transistor operates fully in rectification mode. This creates an inverse relationship (trade-off) between the simulated PAE value and the resulting DC power efficiency.
From the graph above, we know that to achieve the best conversion efficiency in an inverted rectifier power amplifier system, the input power used is actually when the system has the lowest PAE value. This occurs because there is a non-linear (inversely proportional) relationship between PAE and DC power output, which can be seen from the following formula:

$$\text{PAE} = \frac{P_{\text{OUT}} - P_{\text{IN}}}{P_{\text{DC}}} \times 100\%$$

Where:

PAE = Power Added Efficiency (%)
P_{OUT} = RF Output Power (Watt)
P_{IN} = RF Input Power (Watt)
P_{DC} = DC Output Power (Watt)

From the formula above, it can be seen that PAE is inversely proportional to DC power (P_{DC}). Therefore, when the PAE value is low (such as at $P_{in} = 41$ dBm with a PAE of 16.6%), the produced DC power and conversion efficiency will

actually be high (reaching 66.9%). Conversely, if the PAE value is high, the resulting DC power will be lower.

c. Bias Gate Network

The Bias Gate Network functions as a regulator of the transistor's operating voltage so that it can operate under optimal conditions. This system uses a bias voltage of -2.7 V, which determines the quiescent operating point of the CGH40010F transistor.

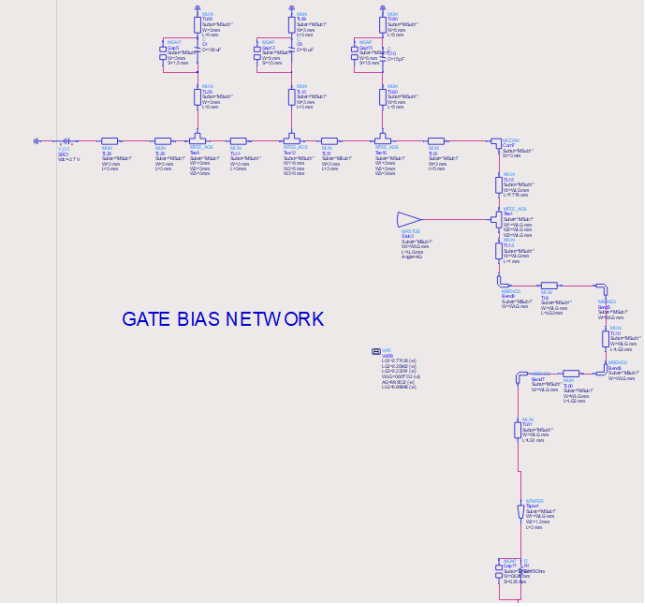


Figure 8. Schematic of Gate Bias Network Rectifier.

This circuit contains three shunt decoupling capacitors, each serving a specific filtering function across different frequency bands. Specifically, the $100\ \mu$F capacitor filters out low-frequency noise and stabilizes the DC voltage source, the $10\ \mu$F capacitor provides mid-frequency decoupling to suppress power supply fluctuations, and the 15 pF capacitor acts as a high-frequency RF bypass filter that isolates the DC bias line to prevent RF signal leakage into the supply source. Additionally, a $\lambda/4$ (quarter-wavelength) transmission line is utilized as an RF choke and impedance transformer, presenting a high impedance (open circuit) to the RF signal path while allowing the -2.7 V DC bias to pass smoothly to the gate terminal of the transistor.

d. Input Matching Network

Input matching networks are designed to transform the standard $50\ \Omega$ source impedance into the optimal input impedance of the transistor determined from source pull and load pull analysis. At high operating frequencies such as 2.6 GHz, distributed microstrip elements are preferred over lumped components to minimize parasitic effects. Impedance matching network design is a critical aspect of RF circuit design, as it ensures maximum power transfer from the source to the load with minimum reflection by matching the source impedance with the complex conjugate of the transistor's input impedance.

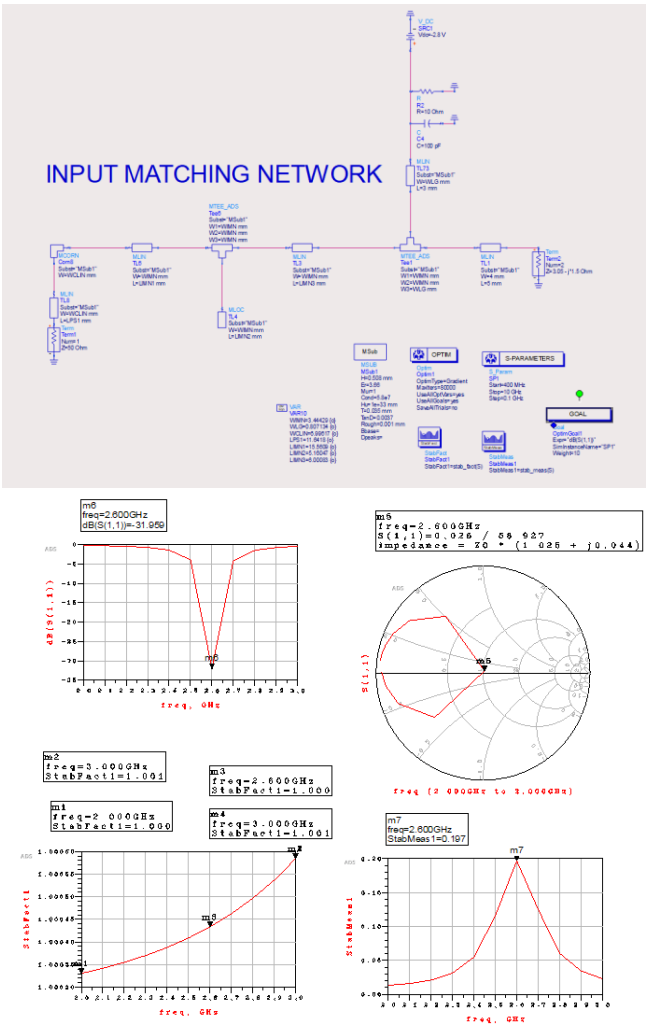


Figure 9. Input Matching Network Schematic

Figure 9 shows the input matching network using microstrip transmission line segments as the primary signal path, combined with stub circuits that function as reactive elements. These distributed microstrip elements work together to transform the standard $50\ \Omega$ RF source impedance into the optimal complex conjugate impedance required by the CGH40010F GaN HEMT gate terminal, thereby maximizing RF power transfer into the device.

e. Output Matching Network

An output matching network functions to transform the output impedance of the transistor to the optimal load impedance, incorporating harmonic termination for high-efficiency inverted Class-F rectifier operation. This network effectively transforms the fundamental and harmonic impedance levels to optimize the RF-to-DC energy conversion performance.

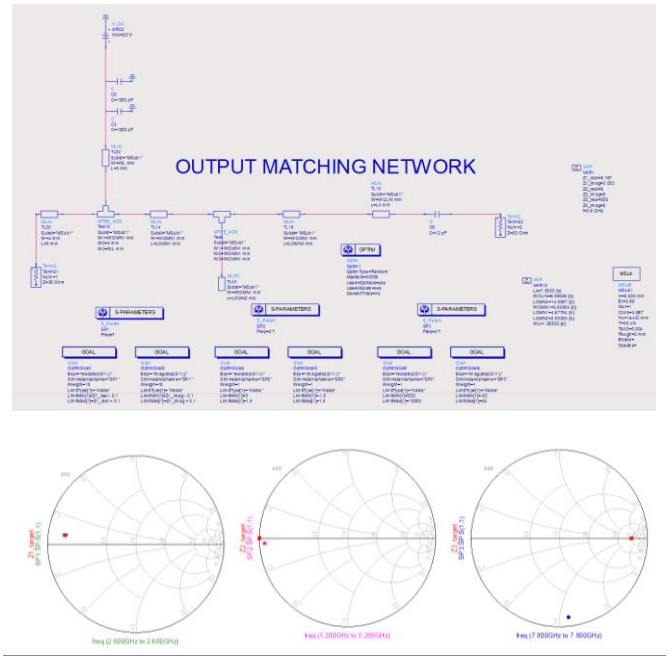
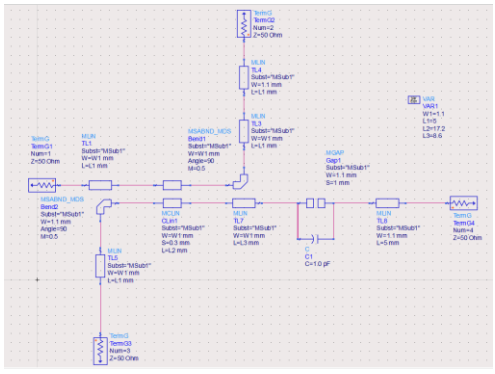


Figure 10. Output Matching Network Schematic

The Output Matching Network design shown in Figure 10 employs a multi-stage matching approach using distributed microstrip transmission lines and stub circuits. The primary signal path consists of series microstrip lines including TL2, TL14, TL16, and TL18, connected through a corner element (Corn10) to TL12. To handle reactive tuning and harmonic control, the network incorporates stub circuits such as TL82 and an open-circuited stub TL93. Physical dimensions of these transmission lines are fully parameterized using variables such as WOMN1, LOMN1, LOMN2, LOMN3, WCLIN, and WL, enabling precise optimization of line widths (W) and lengths (L) to match the transistor output to the target system load.

f. Coupling Directivity

The directional coupler in this RF system functions as a power divider by utilizing electromagnetic coupling between two microstrip transmission lines. When an RF signal is applied to Port 1 (input), the majority of the power flows directly through the main channel to Port 2 (through port), while a small, precise fraction of the power leaks to Port 3 (coupled port) through the electromagnetic field. Port 4 (isolated port) receives minimal power and is terminated to absorb unwanted reflections.



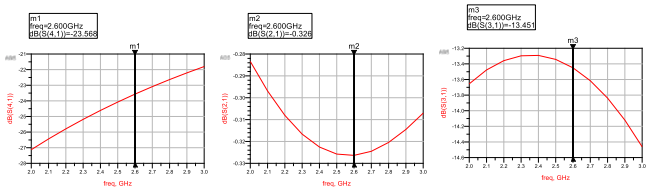


Figure 11. Design schematic directional coupling and Result simulation of the directional coupler.

Figure 11 shows the simulation performance of the microstrip directional coupler at the target operating frequency of 2.6 GHz. The coupling parameter $S(3,1)$, represented by marker m3, achieves a value of -13.451 dB, indicating a loose coupling factor where approximately 4.5% of the input power is sampled to the coupled port. The main line insertion loss $S(2,1)$, shown by marker m2, is only -0.326 dB, demonstrating that over 92% of the input energy passes through the main channel with minimal attenuation. Additionally, the isolation parameter $S(4,1)$, indicated by marker m1, reaches -23.568 dB . This yields a directivity of approximately 10.12 dB (calculated as $|S(4,1)| - |S(3,1)|$), confirming good signal separation between forward and reverse paths while effectively preventing reverse signal interference.

g. Phase Shifter

A phase shifter is a critical component in a switching amplifier circuit that regulates phase in the feedback loop, ensuring system stability and optimal performance. The phase shifter works by receiving a signal from a coupler that samples the amplifier output, then shifting the phase of that signal before comparing it to the reference signal at the input. This precise phase shift ensures that negative feedback operates correctly to maintain the stability and linearity of the amplifier.

The Phase Shifter section in this schematic is a component that functions to regulate or shift the phase of an RF signal without changing the amplitude of the signal. This phase shifter is placed on the lower path of the circuit, connected to transmission lines TL14 and TL15, which indicate its position in the control or feedback path of the system. A phase shifter works by changing the length of the electrical path that RF signals travel through, thereby controlling the phase relationship between input and output signals. This component is essential in applications that require precise phase synchronization

h. Output DC

The DC The DC output in this schematic represents the final stage of the RF-to-DC conversion and filtering process, extracting usable direct current from the rectified high-frequency signal. Instead of relying on lumped inductors, this design utilizes a quarter-wavelength ($\lambda/4$) microstrip transmission line acting as a distributed RF choke. This $\lambda/4$ stub presents a high impedance (open circuit) at 2.6 GHz to block high-frequency RF signals from reaching the output port, while providing a low-resistance path for the extracted DC current. Furthermore, a network of shunt decoupling capacitors is placed along the DC line to filter out residual RF ripple and high-frequency noise, resulting in a stable DC voltage delivered across the $50\ \Omega$ load resistor (R_{DC}).

After all functional elements of the rectifying inverted Class-F power amplifier topology have been individually designed and optimized, the complete system is integrated into a unified final schematic.

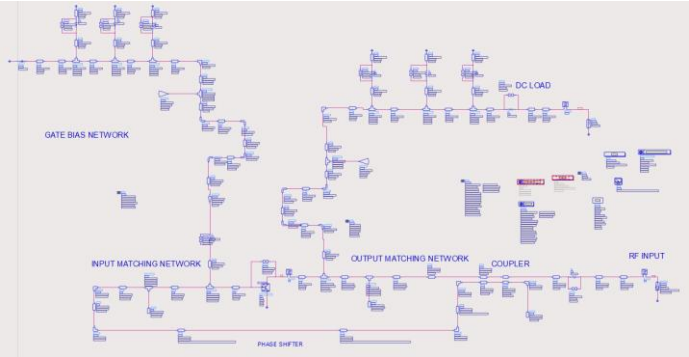


Figure 12. Schematic of the Rectifying of Inverted Power Amplifier Class F.

Figure 12 shows the complete integrated schematic design operating at a center frequency of 2.6 GHz with an RF input power range up to 40 dBm. The system employs a gate bias voltage of -2.7 V to establish the optimal operating point for the CGH40010F GaN HEMT transistor, paired with a 50 Ω DC load termination. Once the schematic circuit is verified to satisfy all electrical requirements and rectifier topology specifications, the design is converted into a physical layout for fabrication.

In this layout conversion stage, the schematic symbols and parameterized microstrip elements are transformed into actual physical geometries, considering fabrication constraints such as trace widths, minimum spacing, and substrate layer properties. In ADS, this process involves optimizing component placement for high-frequency performance and thermal dissipation, routing interconnects smoothly, and designing a continuous ground plane and power distribution network.

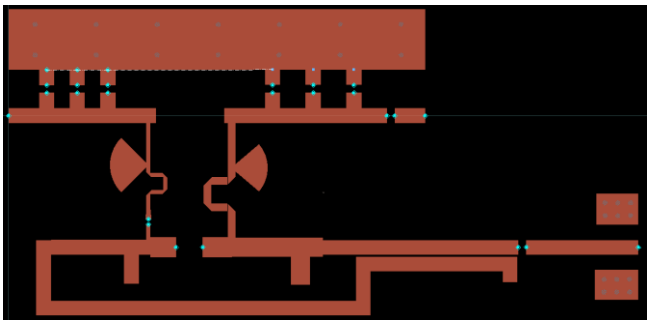


Figure 13. Layout of rectifier inverted power amplifier.

b. Implementation

The PCB (Printed Circuit Board) manufacturing process for rectifiers uses a Rogers RO4350B substrate, which is specifically designed for high-frequency applications. This Rogers RO4350B material has a dielectric constant of 3.66 and a tangent loss of 0.004, which is highly effective in reducing signal loss. The PCB thickness used is 0.508 mm with a copper thickness of 35 um. The manufacturing process produces a PCB with dimensions of 123 mm x 60 mm that meets very tight dimensional tolerances, ensuring optimal quality and compatibility. The microstrip traces, which are the main conductive paths on the PCB for transmitting RF signals, are produced with high precision to maintain a characteristic impedance of 50 ohms. This is crucial for ensuring accurate and stable signal transmission without unwanted interference or reflections. Additionally, the solid ground plane on the PCB serves to provide an optimal signal return path, which is critical for maintaining signal stability and quality. The manufacturing process also includes the creation of accurate via connections and surface finishing in accordance with standards.

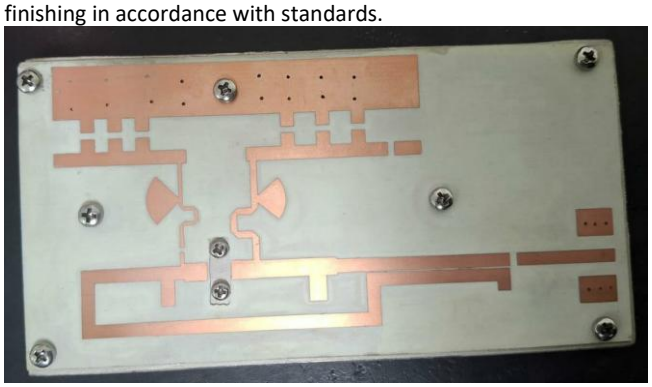


Figure 14. Manufacture PCB Result

This image shows the fabricated RF rectifier PCB designed specifically for the CGH40010F GaN HEMT transistor using Rogers RO4350B substrate. The copper trace structure on the PCB forms a complex stepped impedance matching network pattern, with a multi-level configuration that functions as a step-up impedance transformer from the input to the rectifier output. This design optimizes power transfer from the RF source to the load by minimizing reflection, which is critical for rectifier efficiency. The pad area visible in the center of the PCB is specifically designed for mounting the CGH40010F GaN HEMT transistor, with optimal thermal management considerations given the high power density characteristics of GaN technology. The following image shows the PCB with the components already assembled.

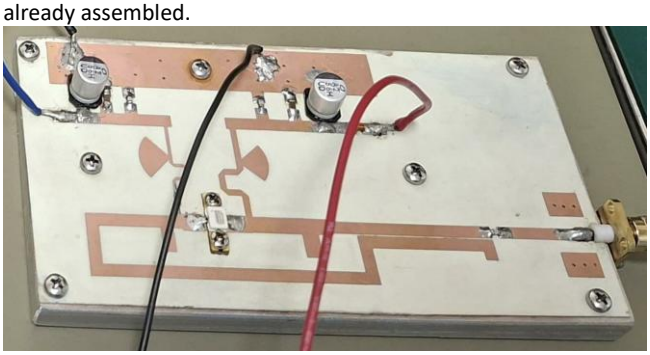


Figure 15. Process Assembly Component Result

III. RESULT AND DISCUSSION

A. Simulation Result

After designing the schematic of the rectifying of inverted power amplifier, the simulation results achieved after the cosimulation optimization process are as follows.

a) Reflection coefficient

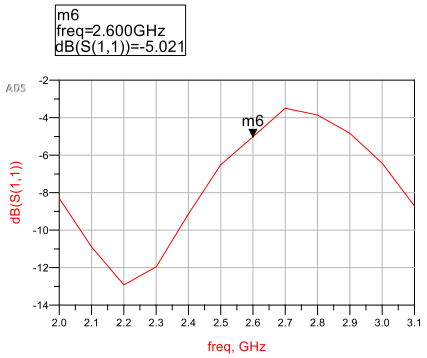
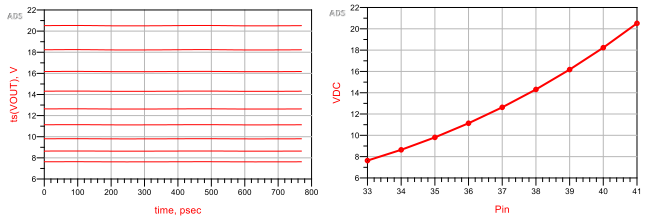


Figure 16. Reflection coefficient Result

Figure 16 shows the simulated input reflection coefficient (S_{11}) at 2.6 GHz, resulting in a small-signal S_{11} value of approximately

-5 dB. Unlike conventional linear amplifiers that strictly require $S_{11} < -10$ dB, high-power rectifiers operate under large-signal conditions. In this design, the input matching network was intentionally optimized at high input power levels (33 dBm to 41 dBm) to achieve maximum RF-to-DC conversion efficiency. As the input power increases to its operational level, the dynamic input impedance of the CGH40010F transistor shifts to its optimal state, allowing efficient energy conversion.

b) Output DC Voltage



(a) **(b)**

Figure 17. (a) Output DC Voltage Waveforms Result (time-domain). (b) Chart Output DC Voltage Simulation Result

Figure 15(a) presents the time-domain waveform analysis of the DC output voltage across a time window from 0 psec to 800 psec for various input power levels from 33 dBm to 41 dBm. The perfectly flat horizontal lines confirm that the converted DC output remains highly stable and free from high-frequency RF ripple across all power levels.

Figure 15(b) illustrates the non-linear relationship between the RF input power (P_{in}) and the generated DC output voltage (V_{DC}) across a 50 Ω load at 2.6 GHz. At a lower input power of 33 dBm, the circuit delivers an output DC voltage of approximately 7.6 V. As the RF input power increases to 41 dBm, the output voltage grows smoothly and continuously, reaching a maximum level of over 20.5 V. This steady increase demonstrates that the output filtering network effectively suppresses high-frequency harmonics while delivering stable DC power without entering premature saturation

c) Output DC Current

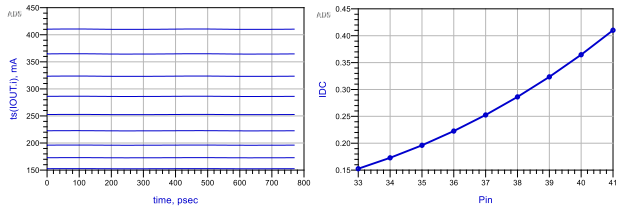


Figure 18.(a) Output DC Current Waveforms Result (time-domain). (b) Chart Output DC Current Simulation Result

Figure 16(a) presents the time-domain waveform analysis of the DC output current (ts(IOUT.i)) across a time window from 0 psec to 800 psec for input power levels swept from 33 dBm to 41 dBm. The flat horizontal lines confirm that the converted DC output current remains extremely stable over time without high-frequency RF ripple. The resulting current levels range from approximately 150 mA (0.15 A) at the lowest input power up to 410 mA (0.41 A) at peak input power.

Figure 16(b) shows the relationship between the RF input power (P_{in}) and the generated DC output current (I_{DC}) across a 50 Ω load at 2.6 GHz. At an input power of 33 dBm, the circuit delivers a DC output current of approximately 0.15 A. As the RF input power increases to 41 dBm, the DC current grows linearly and continuously, reaching a maximum value of 0.41 A (410 mA). This steady current rise demonstrates that the rectifier efficiently conducts high current under large-signal operational conditions without experiencing current saturation.

d) Power Conversion Efficiency

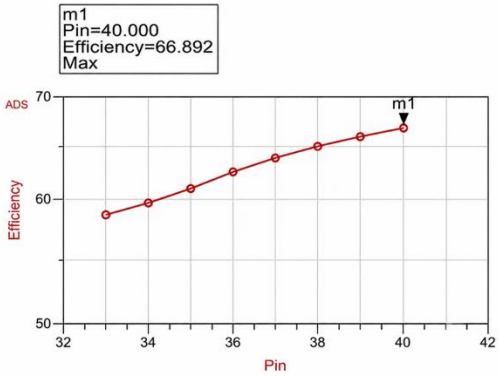


Figure 19. *Simulation results of power conversion efficiency.*

The efficiency curve shown in Figure 17 illustrates the relationship between system efficiency and input power (Pin), with a maximum efficiency of 66.487% achieved at an input power of 40 dBm.

At the starting input power of 33 dBm, the efficiency begins at 58.730%. As the input power increases, the efficiency rises steadily, entering the optimal range above 38 dBm with efficiency values exceeding 64%. The efficiency reaches its peak at 41 dBm (66.487%), demonstrating effective power conversion across the tested input power range.

e) Power Conversion Efficiency vs Power DC

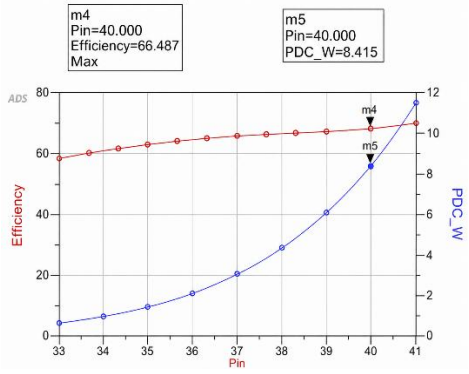


Figure 20. Simulation results of power conversion efficiency vs Output DC Power

This curve presents the relationship between RF input power (Pin), RF-to-DC power conversion efficiency (red curve), and DC output power (blue curve) of the proposed RF rectifier. The conversion efficiency increases gradually as the input power rises, indicating stable rectification performance over the operating range. The efficiency reaches a maximum value of 66.487% at an input power of 40 dBm, demonstrating that the rectifier achieves its optimum operating condition at this input level.

The DC output power also increases significantly with increasing RF input power, exhibiting a nonlinear characteristic. At lower input power levels, only a small portion of the RF energy is converted into DC power because the transistor has not yet reached its optimal switching operation. As the input power increases, the transistor operates more effectively, reducing conduction and switching losses and enabling more RF energy to be converted into useful DC power. At the optimum operating point of 40 dBm, the rectifier produces a

DC output power of 8.415 W while maintaining a power conversion efficiency of 66.487%.
These results indicate that the proposed RF rectifier is capable of maintaining relatively stable conversion efficiency while delivering higher DC output power at increased RF input levels. Therefore, the operating point of 40 dBm represents the best trade-off between conversion efficiency and output power, making the proposed design suitable for high-power RF energy harvesting and wireless power transfer (WPT) applications.

b. Measurement

The testing began with a thorough initial inspection of the manufactured PCB and assembled components to identify any visual defects or soldering irregularities. This was followed by a continuity test using a multimeter to ensure that all electrical connections were intact and to detect any short circuits on the PCB traces.
To obtain accurate and comprehensive measurements, a specific equipment setup was used. An RF Signal Generator was utilized to generate the input RF signal with precisely controlled frequency and power, set at 2.6 GHz, which is the operating frequency of the rectenna. The signal from the generator was then amplified using a driver amplifier stage to supply a total RF input power (P_{in}) of 40 dBm (10 W) to the Class F rectifier circuit based on the CGH40010F GaN HEMT transistor.
To obtain accurate data for calculating conversion efficiency, a Power Meter was employed to measure both the input RF power supplied and the DC output power generated by the rectifier circuit. This measurement is essential for evaluating the overall performance of the system. In addition, the DC output voltage and current were measured using a high-precision Digital Multimeter (DMM) and monitored via programmable DC Power Supply units. A variable load was connected to simulate different operating conditions, allowing analysis of the system's response to load variations.

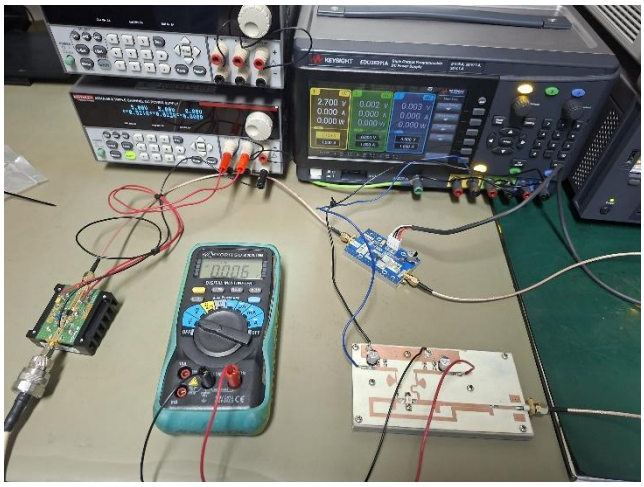


Figure 21. Measurement setup for the Class F RF Rectifier using CGH40010F GaN HEMT transistor at $P_{in} = 40$ dBm and 2.6 GHz

The In the testing of the Class F RF rectifier, conversion efficiency was the primary parameter evaluated. Efficiency was measured as the ratio of the DC output power to the RF input power according to the equation:

$$\eta = \frac{P_{DC\ OUTPUT}}{P_{RF\ INPUT}} \times 100\%$$

The measurement results evaluate the capability of the Class F rectifier using the CGH40010F GaN HEMT transistor to convert high-power RF signals (40 dBm) into DC energy. As observed in the measurement setup, the digital multimeter recorded a DC output voltage reading of 0.006 V (6 mV) during the test.

RF Input (dBm)	POUT_dBm	VDC (mV)
0	0	6
1	1	6
2	2	6
3	3	6
4	4	6
5	5	6
6	6	6
7	7	6
8	8	6
9	9	6
10	10	6
11	11	6
12	12	6
13	13	6
14	14	6
15	15	6
16	16	6
17	17	6
18	18	6
19	19	6
20	20	6
21	21	6
22	22	6
23	23	6
24	24	6
25	25	6
26	26	6
27	27	6
28	28	6
29	29	6
30	30	6
31	31	6
32	32	6
33	33	6
34	-33	6
35	-33	6
36	-34	6
37	-35	6
38	-36	6
39	-36	6
40	-36	6

Table 2. Measured DC Output Voltage (VDC) and RF Power (POUT) versus RF Input Power (Pin).

The power conversion efficiency (η) of the rectifier is defined as the ratio of the output DC power ($P_{DC\ output}$) to the input RF power ($P_{RF\ input}$), expressed as a percentage:

$$\eta = \frac{P_{DC\ OUTPUT}}{P_{RF\ INPUT}} \times 100\%$$

Description:

- η = Rectifier Efficiency (%)
- P_{output} = Output DC Power (Watt)
- P_{input} = Input RF Power (Watt)
- 1. RF Input Power Conversion (P_{input})

For an input power (P_{in}) of 40 dBm, we convert the dBm value into Watts using the formula:

$$P_{input} = 10^{\left(\frac{P_{dBm}}{10}\right)} \times 10^{-3}\ \text{W}$$

$$P_{input} = 10^{\left(\frac{40}{10}\right)} \times 10^{-3}\ \text{W} = 10^{4} \times 10^{-3}\ \text{W} = 10\ \text{Watt} = 10{,}000\ \text{mW}$$

- 2. DC Output Power Calculation ($P_{DC\ output}$)

The DC output power can be calculated using the formula below. Given $V_{DC} = 6\ \text{mV} = 0.006\ \text{V}$:

$$P_{DC\ output} = \frac{V_{DC}^2}{R_{DC}}$$

Description:

- $P_{DC\ output}$ = Output DC Power (Watt)
- V_{DC} = Output DC Voltage (V)
- R_{DC} = Load Impedance (Ω)

With a load impedance (R_{DC}) of 40 Ω, the calculation for $P_{DC\ output}$ is:

$$P_{output} = \frac{(0.006)^2}{40} = \frac{0.000036}{40} = 0.0000009\ \text{W} = 0.9\ \mu\text{W} = 0.0009\ \text{mW}$$

- 3. Rectifier Efficiency Calculation (η)

So, the efficiency can be calculated using the previous formula:

$$\eta = \frac{P_{output}}{P_{input}} \times 100\%$$

$$\eta = \frac{0.0009\ \text{mW}}{10{,}000\ \text{mW}} \times 100\% = 0.000009\%$$

So the efficiency of the rectifier measured with a multimeter at $P_{in} = 40$ dBm is 0.000009% (or $9 \times 10^{-6}\%$).

IV. ANALYSIS AND CONCLUSION

This research demonstrated the design and simulation of a high-efficiency GaN-based RF rectifier system using an inverted Class F RF power amplifier topology for wireless battery charging systems. The developed rectifier circuit, implemented with the CGH40010F GaN HEMT transistor on a Rogers RO4350B substrate, represents a significant advancement in wireless power transfer technology. The integration of critical components including the microstrip coupler, phase shifter, and transmission line-based impedance matching networks successfully converts the GaN HEMT Class F power amplifier into an efficient synchronous rectifier based on time reversal duality principles.

The comprehensive design methodology employed in this study, combining theoretical analysis, circuit optimization, and performance simulation, has yielded exceptional theoretical results. The rectifier system operates at 2.6 GHz with a nominal input power of 40 dBm (10 W). However, the physical implementation results revealed a significant performance discrepancy compared to the simulation targets, where the measured DC output voltage reached only 6 mV (0.006 V).

The contrasting results between simulation and physical implementation reveal a significant gap that requires an in-depth analysis of the non-ideal factors during the realization and measurement processes:

No	Performance Degradation Factor	Physical Root Cause	Impact on RF/DC Performance
1	Suboptimal Etching Temperature	Chemical etching solution was insufficiently heated during PCB fabrication, causing incomplete copper removal (under-etching) and trace edge roughness.	Alters microstrip trace geometry (width and length), changing the characteristic impedance (Z_0) and causing severe power reflection at 2.6 GHz.
2	Substrate-Process Incompatibility at TFME	Manufacturing processes and chemical formulas at the TFME facility are standardized for FR-4 substrates rather than high-frequency Rogers RO4350B material.	Introduces physical dimensional tolerances and conductor imperfections, leading to RF signal degradation across the transmission lines.
3	DC Load Component Limitation	Availability constraints for a dedicated 50 Ω RF resistor component at the DC Load output stage during testing.	Prevents the circuit from operating at its optimal load line, causing severe impedance mismatching and dropping the

B. Conclusion

This research successfully designed and implemented a GaN HEMT CGH40010F-based RF rectifier system using an inverted Class F power amplifier topology on a Rogers RO4350B substrate for wireless battery charging applications. The system was designed to operate at 2.6 GHz frequency with 40 dBm (10 W) input power using a comprehensive methodology that integrates microstrip coupler, phase shifter, and impedance matching networks based on time reversal duality principles.

Simulation results demonstrated high power conversion performance under ideal operating conditions. However, hardware implementation experienced significant degradation, resulting in a measured DC output voltage of 6 mV (0.006 V). This discrepancy was primarily caused by non-optimal PCB fabrication processes due to insufficiently heated chemical etching solutions, process incompatibility at the TFME fabrication facility (where standard parameters and formulas are optimized for FR-4 substrates rather than high-frequency Rogers RO4350B materials), and component availability limitations regarding the 50 Ω RF resistor at the DC load terminal.

This research proves the potential of GaN-based Class F RF rectifier technology for wireless power transfer and contributes a design methodology for developing wireless battery charging systems. Despite the gap between simulation and physical realization, these experimental findings provide essential engineering insights and serve as a practical foundation for future optimizations in high-power wireless charging technology.

Future research needs to focus on optimizing PCB fabrication processes with strict temperature and chemical etching controls specifically tailored for high-frequency Rogers substrates, securing dedicated high-power 50 Ω RF load components for measurements, and refining layout co-simulations to minimize the simulation-implementation gap. Implementation of systems at a practical scale for real-world wireless charging applications and integration with intelligent power management systems are also required. From a fundamental perspective, deeper investigation into time reversal duality principles and exploration of other frequency bands will open broader application opportunities for wireless power transfer technology.

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FORMULIR LOOGBOOK BIMBINGAN DAN PENGAJUAN
SEMINAR PROPOSAL/SIDANG TUGAS AKHIR/ PROYEK AKHIR*

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NIM : 3222301007
Pembimbing I : Dr. Ir. Basuki Rachmatul Alam
Pembimbing II* : -
Judul : Design and Implementation of High Conversion Efficiency RF to DC Rectifier Based on Inverted Gate Topology of Class F GaN HEMT RF High Power Amplifier

No	Hari/Tgl	Rincian Kegiatan	TTD Pembimbing I & II	
1	Rabu, 11 Februari 2026	Rencana perancangan terkait penelitian kedepan setelah selesai revisi seminar proposal.		
2	Jumat, 13 Februari 2026	Membahas perancangan skematik RF-to-DC Rectifier dan desain awal impedansi matching network (input/output).		
3	Rabu, 06 mei	Pembahasan terkait perencanaan karakteristik dan pemilihan jenis komponen transistor GaN HEMT yang dipakai.		
4	Rabu, 03 Juni 2026	Mendiskusikan desain dan optimasi microstrip coupler serta phase shifter		
5	Senin, 15 Juni 2026	Membahas Simulasi DC I-V Characterization GaN HEMT dan penentuan operating point (bias point) untuk kestabilan topologi Class F.		
6	Senin, 22 Juni 2026	Diskusi terkait target capaian dari desain layout, Efisiensi dan Parameter		
7	Rabu, 08 Juli 2026	Mendiskusikan untuk membuat design rectifier menggunakan Tansistor CGH40010F 10 Watt		
8	Jumat, 10 Juli 2026	Membahas capaian semua tahapan desain yang telah dibuat dan lanjut untuk menyiapkan jurnal TA		
9	Kamis, 22 Juli 2026	Membahas revisi terkait jurnal Proyek Akhir yang sudah dibuat		
10	Jumat, 24 Juli 2026	Membahas terkait jurnal Proyek Akhir yang sudah dibuat untuk gladi resik dan untuk di sidangkan pada Selasa 28 Juli 2026		

Berdasarkan hasil bimbingan yang telah dilaksanakan selama 3 bulan dan telah disetujui oleh dosen pembimbing, maka dengan ini saya mengajukan diri sebagai peserta ~~Seminar Proposal~~ /Sidang Tugas Akhir/ Proyek Akhir*.

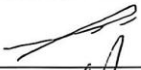
Batam, 24 Juli 2026
Peserta

Grace Liyanti Sitinjak

**Hapus yang tidak perlu.*
Jumlah bimbingan minimal 10 kali. Dalam satu minggu maksimal bimbingan yang dihitung adalah 2 kali.

Job Assignment Matrix

Company Name : TFME (Teaching Factory Manufacturing of Electronics) Politeknik Negeri Batam.
Department : Radio Frequency Laboratory.
Effective Date : 15 September 2025 – 14 September 2026.

No.	Employee Name	Department	Job Title	Assigned Work / Responsibility
1.	Dr. Ir. Basuki Rachmatul Alam	Manufacturing Electronic Engineering (RF Semiconductor)	Lecturer & Mentor	
2.	Grace Liyanti Sitinjak	Radio Frequency Laboratory	Design & Manufacturing Procces RF	

Prepared By	Approved By
Name: Grace Liyanti Sitinjak **Position:** Internship Student **Date:** 13 Agustus 2026	**Name:** Dr. Ir. Basuki Rachmatul Alam **Position:** Lecturer & Mentor **Date:** 13 Agustus 2026

No.FO.31.6.1-V1 Format Pernyataan Publikasi Mahasiswa
14 Juli 2023

Yang bertanda tangan di bawah ini :

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NIM	: 3222301007
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No. Telp	: (0778) 469858

Bersama ini saya sampaikan 1 (satu) set Tugas Akhir/Skripsi/Artikel Penelitian dengan judul:
"Design and Implementation of High Conversion Efficiency RF to DC Rectifier Based on Inverted Gate Topology of Class F GaN HEMT RF High Power Amplifier for Wireless Power Transfer"
"Desain dan Implementasi Penyearah RF ke DC Efisiensi Konversi Tinggi Berbasis Topologi Gerbang Terbalik pada Penguat Daya Tinggi RF Kelas F GaN HEMT untuk Transfer Daya Nirkabel"

Saya sebagai penulis menyatakan memberikan hak sepenuhnya kepada Politeknik Negeri Batam dengan ketentuan**:

- ☑ Mempublikasikan naskah dalam bentuk Tugas Akhir/Skripsi/Artikel Penelitian secara langsung dan menyeluruh.
- ☐ Menunda publikasi naskah Tugas Akhir/Skripsi/Artikel Penelitian sampai dengan ..... tahun terhitung mulai tanggal penyerahan naskah, dan selanjutnya dapat dipublikasikan sesuai dengan ketentuan yang diinginkan.
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Demikian pernyataan ini saya buat dengan sesungguhnya, dan saya bersedia menerima segala risiko, apabila di kemudian hari terbukti pernyataan saya tidak benar.

Batam, 13 Agustus 2026

Yang menyatakan	Instansi/Perusahaan Tempat Pengambilan Data***	Mengetahui Dosen Pembimbing
(Grace Liyanti Sitinjak)	(Dr. Ir. Basuki Rachmatul Alam)	(Dr. Ir. Basuki Rachmatul Alam)

*Jika ada
**Checklist salah satu

*** Keterangan:
1. Tempat penelitian wajib dimasukkan apabila data diambil dari perusahaan
2. Tanda tangan Instansi dapat diberikan oleh Dosen Pembimbing jika Instansi/Perusahaan tempat pengambilan data tidak ada.