Analysis Process Requirement After Safe Launch at Die Attach Process Focused on Package LDSO-14-2

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Abstract— **Safe Launch is used in the semiconductor IC industry to describe and validation process before the final product is launched to production. In author department,the Process Integrated Department (PI) have responsbility to ensure the product meets all specified requirements. Die attach also known in semiconductor industry as die bonding, it is the process attaching die onto the leadframe. At Infineon, when a new product is about to be launched, PSFLA monitoring will be conducted. Products in PSFLA will be run with a production environment and will be assessed for each process, from pre-assembly to MSP test. In this project, the author will focus on the SFLA process of package LDSO-14-2 at Die Attach Process. Author must ensure that this package must meet the specifications and can be used and applied at PT Infineon Batam. For this project, the method of analysis used is box plot and pareto chart, after the safe launch of the die attach process has been carried out, the author can collect data and analyze related to the title of this project.**

Keyword: Die Attach , LDSO-14-2 , Safe Launch

I. Introduction

Die attach is an important process of semiconductor assembly by attaching the die from the wafer to die pad or substrate. Die attach is one of critical processes because there criteria that must be achieved according to spesifications. Before the chip or die attached to die pad,the die pad must first be given a adhesive materials such epoxy or glue. The adhesive is applied with sufficient and controllable quantities.Then, the ejector needle with a predetermined amount will push the chip or die from the bottom of the wafer. The rubber collet also known as pick and place tools,is used to remove the die from the wafer to die paddle. [1]

Ejector needle parameters must be adjusted correctly. When adjusting ejector parameters that are not correct, then potential die cracks will occur.Fillet height in the die attach process refers to the height of the adhesive glue covering the sides of the chip. After the pick and place process is complete, we must ensure that the epoxy or glue coverage on the chip meets the criteria. [2]

Package LDSO-14-2 is a the first package that using the stripmap.At Infineon, when a new product is about to be launched, PSFLA monitoring will be conducted. The purpose of this monitoring is to ensure that the product is ready to be released to production. Products in PFSLA will run with a production environment and will be assessed for each process, from pre-assembly to MSP test. Package LDSO-14-2 has several required quality responses consisting of BLT, die tilt, glue coverage, die shear, voids, and other defects and author must ensure that this package must meet the specification and can be used and applied at PT Infineon Batam. [3]

At Batam site,backend area consists of 3 main processes, namely pre-assembly, assembly, and testing. In the early stages of pre-assembly, the process involves coating the wafer using uv tape, followed by cutting the wafer into individual chips. The chips are then tested through the inspection process. After the pre-assembly process is complete, the next stage is Front of Line. This stage includes the Die attach process, which is attaching the die on a surface and wire bonding the die. The next stage involves the leadframe containing the chip, which is then encapsulated in the molding process and cut to get a package shape known as IC packaging. These stages are part of the complex semiconductor manufacturing process and are critical in ensuring the quality and functionality of the resulting electronic components.

II. Method

Every new product introduction, one of which is LDSO-14-2, involves several stages to be performed. The qualification stage is carried out responsibly by the Development department, the next task will be handed over to the PI department to perform the PSFLA stage. Proses Integration department also conducts planning and scheduling related to lot build which includes the allocation of man power, machines, schedules per process, and other resources,and UPE or EE department has responsibilities related to document updates, tolling and part endorsements, and shopfloor briefings.

A. Flowchart

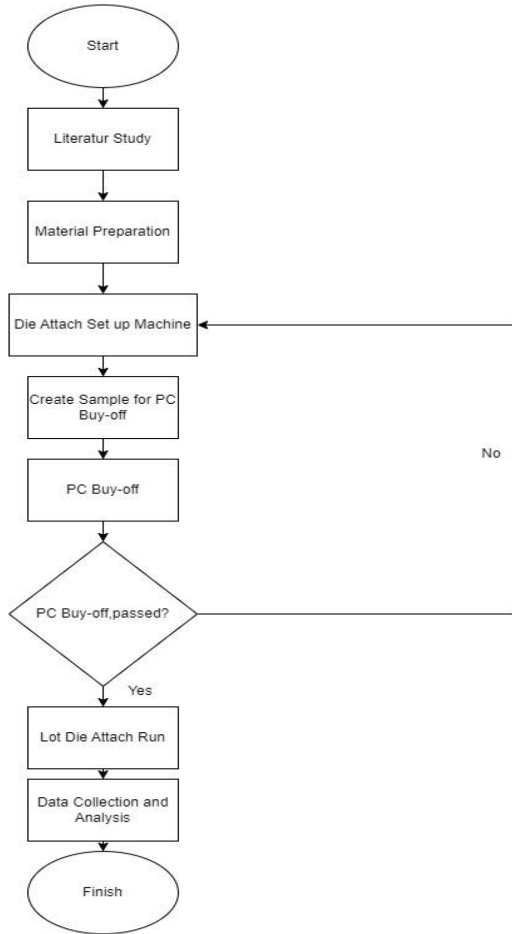

Figure 1. Flowchart

1. Conduct a literature study first to understand all aspects required in the die attach process.
2. After the literature study is complete, prepare the materials that will be used for setting up in the die attach process, such as change nozzle and rubber collet.
3. After the material preparation is complete, before the safe launch process, the set-up machine must be done first and adjusted to the parameters with the device that we will run.
4. After the machine has been set up, make a sample for PC buy-off to ensure the materials and parameters match the criteria.
5. Check the results of the PC buy-off. If the results pass (YES), then we can proceed to the next stage.
6. The next step is data collection and analysis. In this stage, we will collect data and analyze the data we obtain to ensure that the die attach process is running properly and in accordance with the predetermined standards.

B. Machine and Tools

1) ESEC 2100 HSI

The machine used in PFSLA Die attach is Die Attach Glue ESEC 2100 hSi. This machine becomes the machine that will be used in the safe launch process with the predetermined machine settings parameters.

2) KEYENCE

The Keyence VHX is an all-in-one microscope that incorporates observation, image capture, and measurement capabilities. Any user, regardless of their experience, can now obtain high-quality, fully focused images in an instant. For LDSO-14-2 Pre Safe Launch Keyence used for workmanship data collection. [4]

3) HISOMET

The Hisomet is a precision measuring microscope that utilizes an optical focal point detection system, enabling non-contact depth measurement. It features a precise focus indicator that allows for easy measurement of height, depth, and steps by aligning two halves of an index graticule while observing the surface of the object.

C. Data Collection

To collect output response data on LDSO-14-2 package in die attach process using production machines, namely hisomet, keyence, and dage machines. The data taken are bond line thickness, die tilt, die shear, glue voids, and glue coverage with minimum samples taken is 10 units. Each sample strip has 20 columns and 5 rows and total of units for this package are 100 units. Measurement is taken randomly both for column and rows. [5]

R\C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1																				
2																				
3																				
4																				
5																				

Figure 2. Mapping Matrix LDSO-14-2

After safe launch carried out, the output response data collection on the LDSO-14-2 package is divided into main chips and sub chips, which each chip to be bonded uses a different machine.

D. LDSO-14-2 Bonding Diagram

Before configuring the machine with the device to be run,it is important to prepare the material by changing the tool according to be requirements of device,such as changing nozzle or changing rubber collet.The package used for this project is LDSO,which consist of 100 unit divided into 5 rows and 20 columns. Bonded lead frames that used has the bonding diagram as shown below:

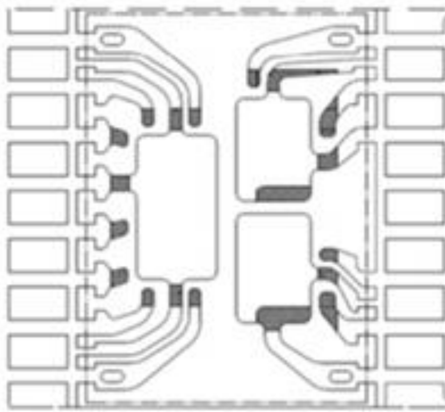

Figure 3. LDSO Bonding Diagram

E. Measurement

For Safe Launch in the Die Attach process monitoring 8 lots and ensuring process requirements on BLT, Die tilt, Die Shear, Glue void and coverage must meet specifications and can run well in production. Running with 2 machines that distribute main chips and sub chips and also have a different specification of measurement.

Table 1. Measurement for main chip

Response	Specs	Max	Min	Average	Stdev	RESULT
BLT	1-10um	3.10	7.77	7.59	0.93	Pass
Die Tilt	Max. 10um	1.10	8.25	3.48	1.90	Pass
Single glue voids	Max. 10%	0	0	0	0	Pass
Total Glue voids	Max.20%	0	0	0	0	Pass
Glue coverage	Min.75% around perimeter	100%	100%	100%	100%	Pass
Die Shear	Min. 6N/mm2	14.4	28.85	23.17	3.36	Pass

From Table 1, it can be concluded that each response output from the die attach process meets the set specifications. The table shows that each process requirement, including bond line thickness, die tilt, single glue voids, total glue voids, glue coverage, and die shear, did not fail and all met the specification values. In addition, a value of 0 in glue voids indicates that there is no issue with glue voids, while 100% in glue coverage indicates that the die is fully covered with glue.

Table 2. Measurement for sub chip

Response	Specs	Max	Min	Average	Stdev	RESULT
BLT	1-10um	4.57	9.28	6.82	1.17	Pass
Die Tilt	Max. 10um	0.60	8.25	2.97	1.98	Pass
Single glue voids	Max. 10%	0	0	0	0	Pass
Total Glue voids	Max.20%	0	0	0	0	Pass
Glue coverage	Min.75% around perimeter	100%	100%	100%	100%	Pass
Die Shear	Min. 6N/mm2	13.77	30.06	24.47	3.21	Pass

From Table 2, it can be concluded that each response output from the die attach process meets the set specifications for sub chip LDSO-14-2. The table shows that each process requirement, including bond line thickness, die tilt, single glue voids, total glue voids, glue coverage, and die shear, did not fail and all met the specification values. In addition, a value of 0 in glue voids indicates that there is no issue with glue voids, while 100% in glue coverage indicates that the die is fully covered with glue.Fillet height is refers to height of the adhesive glue covering the side of the chip.Bond line thickness is thickness between chip and die surface. [6]

III. RESULT AND DISCUSSION

For doing this project, there are several specifications need to be passed by the result to be capable. Table 1 & 2. shown the specification every output response of die attach process. The results of these measurements will help author in evaluating product quality and the overall production process.By using statistical tools,author can calculate relevant statistical values to obtain accurate information from BLT measurements. Data collection on the LDSO-14-2 package is divided into main chip and sub chip.

A. Bond Line Thickness

The data have been taken for BLT which 10 units or chips per lot. Figure 4 & 5 shows the boxplot of the bond line thickness for both chip result.From the boxplot,the distribution of data can be seen still within the upper and lower specification limits,the data distribution still meets th criteria set out in the spesification.BLT have minimum specs 1um and maximum specs is 10um. [6]

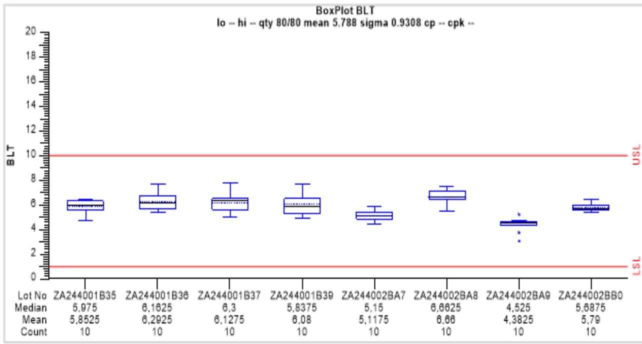

Figure 4. Bond Line Thickness for main chip

Based on specification at Table 2 it can be seen the spesification of bond line thickness with lower limit is 1 um and upper limit is 10 um, from figure 4 the distribution of data shown still in the spesification and and the value of the bond line thickness which is maximum value,minumum value,average,and standard deviasion for the main chip of each lot meets the standard criteria that have been set. [7]

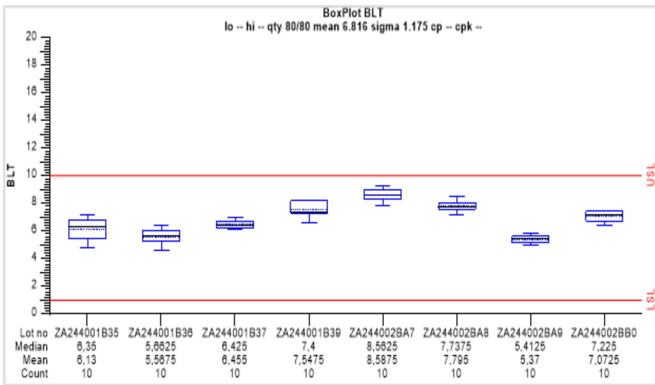

Figure 5. Bond Line Thickness for sub chip

Based on specification at Table 3 it can be seen the specification of bond line thickness with upper limit is 10 um, from figure 5 the distribution of data shown still in the specification and and the value of the bond line thickness which is maximum value, minimum value, average, and standard deviation for the main chip of each lot meets the standard criteria that have been set. [6]

B. *Die Tilt*

The data have been taken for Die Tilt which 10 units or chips per lot. Figure 6 & 7 shows the boxplot of the die tilt for both chip result.From the boxplot,the distribution of data can be seen still within the upper specification limits,the data distribution still meets th criteria set out in the spesification.

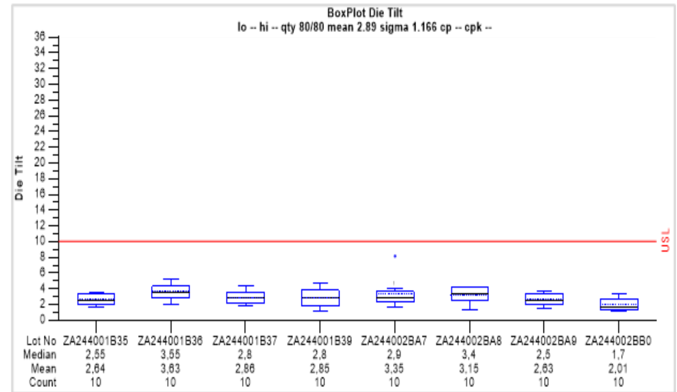

Figure 6. Die Tilt for main chip

Based on specification at Table 1 it can be seen the specification of Die Tilt with upper limit is 10 um, from figure 6 the distribution of data shown still in the specification and and the value of the Die Tilt which is maximum value, minimum value, average, and standard deviation for the main chip of each lot meets the standard criteria that have been set.

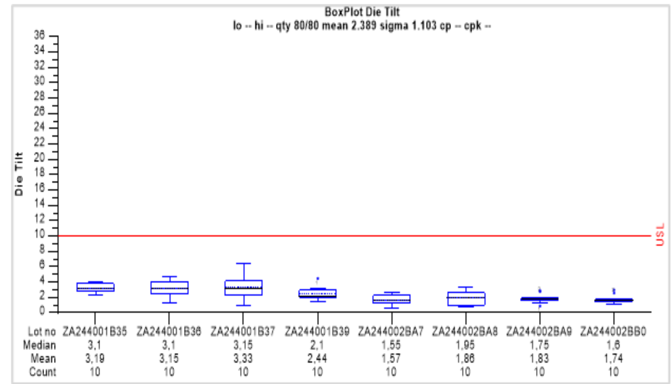

Figure 7. Die Tilt for sub chip

Based on specification at Table 2 it can be seen the specification of Die Tilt with upper limit is 10 um, from figure 7 the distribution of data shown still in the specification and and the value of the Die Tilt which is maximum value, minimum value, average, and standard deviation for the main chip of each lot meets the standard criteria that have been set.

C. *Die Shear*

The data have been taken for Die Shear which 10 units or chips per lot. Figure 8 & 9 shows the boxplot of the die shear for both chip result.From the boxplot, the distribution of data can be seen still within the lower specification limits,the data distribution still meets th criteria set out in the spesification.

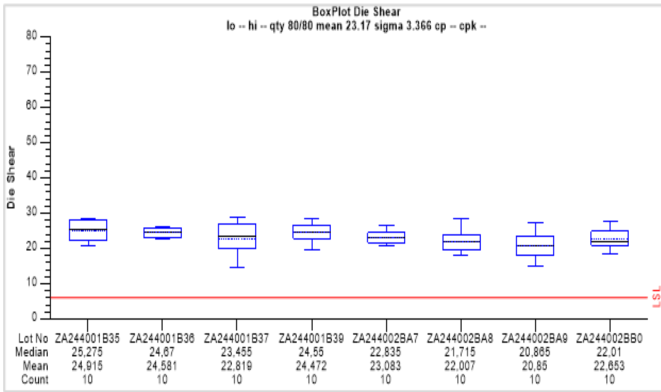

Figure 8. Die Shear for main chip

Based on specification at Table 1 it can be seen the specification of Die Shear with minimum value is 6N/mm2, from figure 8 the distribution of data shown still in the specification and and the value of the Die Shear which is maximum value, minimum value, average, and standard deviation for the main chip of each lot meets the standard criteria that have been set.

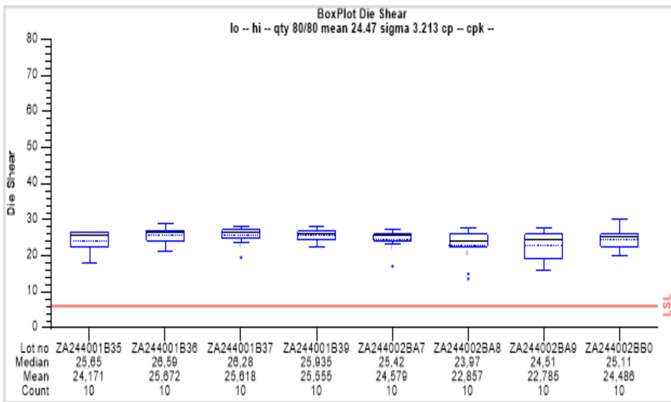

Figure 9. Die Shear for sub chip

Based on specification at Table 1 it can be seen the specification of Die Shear with minimum value is 6N/mm2, from figure 9 the distribution of data shown still in the specification and and the value of the Die Shear which is maximum value, minimum value, average, and standard deviation for the main chip of each lot meets the standard criteria that have been set.

D. *Glue Coverage & Glue Voids*

For glue coverage and glue voids, the criteria shown can be seen by visual inspection. Glue coverage readings are pass (100% coverage) for both chips and glue voids are pass (zero void for glue void single and total) for both chips. [8]

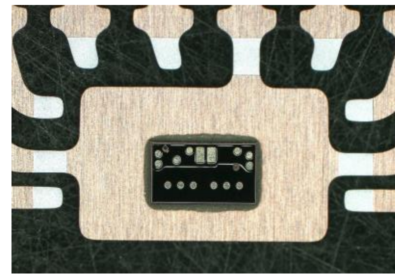

Figure 10. Die Coverage mainchip

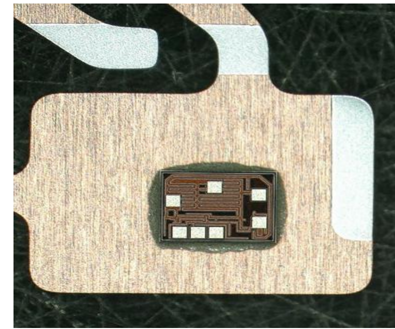

Figure 11. Die Coverage subchip

From figure 10 & 11 , for glue coverage on this package, it can be seen that the die or chip is 100% covered, which means that the requirement for die attach glue coverage passes the criteria. [5]

E. *Defect Pareto*

From Figure 12 on the defect Pareto chart, the highest contribution at Pre-Safe Launch stage is seen in the insufficient glue issue. This allows improvement team to clearly identify that the main focus of improvement should be given to that issue in order to achieve significant improvements in the overall results. [9]

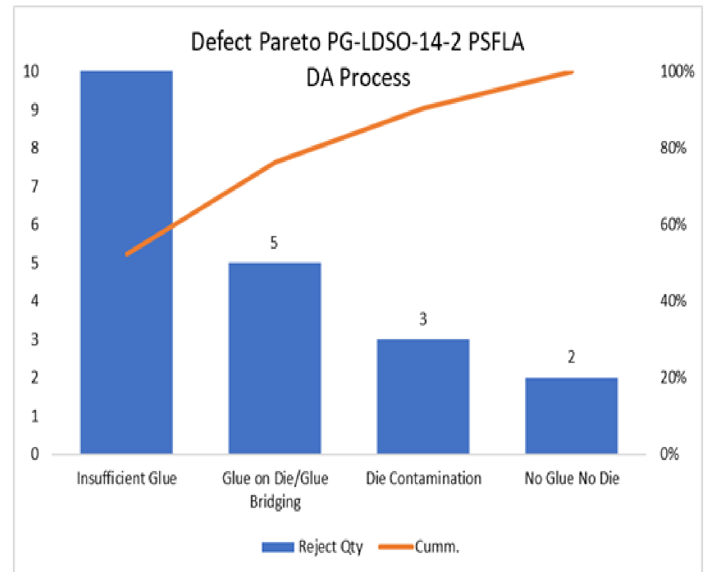

Figure 12. Pareto Defect list

Based on verification the insufficient glue was due to wrong purging setting without pre-dispense after purging. This caused inconsistent glue amount due to the glue built up at the nozzle tip.

IV. CONCLUSION

Based on the result of the research on this project,it can be concluded that the objective of this project research can be achieved after monitoring 8 lot during safe launch for package LDSO-14-2. From the specifications that have been set infineon package has been run pre safe launch to see the results of the process requirements in the die attach process the result is reach the specifications that have been set All 8 lots of package LDSO-14-2 passed the process requirement on BLT,Die Tilt,Die Shear,Glue void and glue coverage and based on Die Attach Requirement Package LDSO-14-2 is fit to be released to production.

V. REFERENCE

[1] PT. Infineon Technologies . “Die Attach Introduction,Module 1.”

[2] PT. Infineon Technologies. “Die Attach Introduction,Module 2.”

[3] PT. Infineon Technologies. “Die Attach Basic Training.”

[4] Military+Aerospace Electronics”Keyence VHX 5000”. Internet : https://www.militaryaerospace.com/directory/electro-optics/optical-imaging/product/14063794/keyence-corp-of-america-vhx5000-digital-microscope

[5] PT. Infineon Technologies.”Front of Line Training.”

[6] Material interview, PT. Infineon Technologies Batam, Kota Batam, 2022, DID Document.

[7] Reni Permata Sari,Ma’rufah Hayati MT. 2019. "Analisis Jumlah PenerimaanPajak Bumi dan Bangunan di Kecamatan Gunung Labuhan Way Kanan". Jurnal Teori dan Aplikasi Matematika (JTAM) No.1: 22-26

[8] Material interview, PT. Infineon Technologies Batam, Kota Batam, 2022, DID Document.

[9] Defect Catalogue, PT. Infineon Technologies Batam, Kota Batam, 2022, Z8R00002132.