Design and Implementation of a High-Power and High-Efficiency RF Class-E Parallel Amplifier with Hybrid Coupler Using GaN HEMT Transistors for Wireless Power Transfer

Final Project Proposal

By:
M. Adha Alhafiz (3222311035)

Electronics Manufacturing Engineering Study Program
Electrical Engineering Department
Politeknik Negeri Batam
2026

Statement of Authenticity of Final Project

I, the undersigned, hereby declare that the contents of my Final Project, entitled: **"Design and Implementation of a High-Power and High-Efficiency RF Class-E Parallel Amplifier with Hybrid Coupler Using GaN HEMT Transistors for Wireless Power Transfer",** are entirely my own work, compiled without the use of unauthorised materials, and do not constitute the work of any other party which I have claimed as my own. All sources cited or referred to in this work have been fully listed in the bibliography. Should this declaration prove to be untrue at a later date, I am willing to accept sanctions in accordance with the applicable regulations.

Batam, 30 July 2026

M. Adha Alhafiz
NIM: 3222311035

Approval sheet

The Final Project is structured to fulfill one of the requirements for obtaining a degree
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By:
M. Adha Alhafiz (3222311035)

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Approved by:

Examiner I:
Muhammad Arifin, S.Si., M.Si.
NIK: 116161

Supervisor:
Dr. Ir. Basuki Rachmatul Alam
NIK: 122274

Examiner II:
Prasaja Wikanta, S.T., M.T.
NIK: 103026

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ABSTRACT

Rapid advances in wireless energy technology have increased the demand for highly efficient RF power amplifiers capable of handling high power for Wireless Power Transfer (WPT) systems. This study presents the design and implementation of a high-power RF amplifier based on a parallel Class-E topology that integrates a hybrid power combiner, using GaN HEMT transistors. The proposed architecture aims to overcome the power capacity limitations of a single Class-E amplifier by connecting multiple transistors in parallel and combining their outputs through a low-loss -3 dB hybrid combiner, allowing for a higher total output power while maintaining excellent operational efficiency and stability. GaN HEMT transistor technology is applied due to its superior electrical and thermal properties, such as high breakdown voltage, high current density, fast switching operation, and better thermal resistance. These characteristics make GaN devices suitable for Class-E operation at high voltages (28 V) with output power above 10 W and power added efficiency (PAE) exceeding 80%. The comprehensive design process includes non-linear device modeling, Class-E load network synthesis, hybrid coupler optimization, impedance matching, and electromagnetic co-simulation using Advanced Design System (ADS). This power amplifier is implemented on a Rogers RO4350 20 mils substrate with a PCB layout optimized for current distribution, minimal input loss, phase symmetry, and thermal management. Practical measurements confirm efficient power combining, stable amplifier operation under load variations, and reliable thermal performance under continuous high-power conditions. The developed amplifier offers a practical and scalable solution for high-power WPT transmitters that can be used in wireless electric vehicle charging, UAV power transmission platforms, and renewable energy distribution systems in remote areas, setting a new standard in RF efficiency, power density, and operational reliability.

Keywords: ***High Power Amplifier, Class-E Parallel Topology, Hybrid Coupler, GaN HEMT, Wireless Power Transfer, High Efficiency.***

FOREWORD

The author expresses gratitude to Almighty God for His mercy and guidance, enabling the author to successfully complete this final project entitled "Design and Implementation of a High-Power and High-Efficiency RF Class-E Parallel Amplifier with Hybrid Coupler Using GaN HEMT Transistors for Wireless Power Transfer." The writing of this final project is one of the academic requirements for completing the Manufacturing Electronics Engineering study program at Batam State Polytechnic.

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11. All parties that the author cannot mention one by one, who have provided assistance in any form during the process of preparing this final project.

The author realizes that this final project is far from perfect. Therefore, the author welcomes constructive criticism and suggestions from all parties in order to improve this final project. Hopefully, this final project can contribute to the development of science and technology for readers in general.

Batam, 22 Juli 2026

M. Adha Alhafiz

Design and Implementation of a High-Power and High-Efficiency RF Class-E Parallel Amplifier with Hybrid Coupler Using GaN HEMT Transistors for Wireless Power Transfer

M. Adha Alhafiz[1], Basuki Rachmatul Alam[2]

Teaching Factory Manufacturing of Electronics, Politeknik Negeri Batam,
Jl. Ahmad Yani, Batam Center, Batam 29461, Provinces of Riau Island, Indonesia
E-mail: basuki@polibatam.ac.id

***Abstract*— This paper presents the design, implementation, and analysis of a high-power RF Class-E parallel power amplifier integrated with a hybrid coupler for 2.6 GHz wireless power transfer (WPT) applications. To overcome the output power limitations of a single Class-E amplifier, a parallel topology utilizing two GaN HEMT transistors is proposed, with outputs combined through a 3dB hybrid coupler. The system was designed and verified using electromagnetic (EM) co-simulation to account for parasitic effects on a Rogers RO4350 substrate (20 mils thickness). These characteristics make GaN devices suitable for Class-E operation at high voltages (28V) with integrated parallel amplifier achieves a total output power of 17.419 W (42.410 dBm) and a total DC power consumption of 12.693 W with a large-signal gain of 18.511 dB and a drain efficiency of 68.617% and power added efficiency (PAE) 63.658% at 2.6 GHz, operating with a total input power of 31 dBm. The fully integrated parallel PCB implementation is designed compactly with dimensions of 155.874 mm × 93.083 mm, confirming the feasibility of this balanced architecture design. This work advances high-efficiency RF power amplification technology, particularly for wireless power transfer systems where scalability and energy efficiency are paramount. The results demonstrate the potential of parallel Class-E GaN-based amplifiers to enable high-power wireless energy transmission, with important implications for applications ranging from electric vehicle charging to remote power distribution systems.**

Keywords: ***HPA, Hybrid Coupler, Class E, GaN HEMT, PAE, Pdc, DE, Pgain, Pdel dBm.***

I. INTRODUCTION

Wireless Power Transfer (WPT) is a method of transmitting power wirelessly through electromagnetic waves, eliminating the need for physical connections. In long-distance Radio Frequency Wireless Power Transfer (RF-WPT) configurations, electrical energy is converted into RF signals, emitted by a transmitting antenna, propagates through free space, and is then captured and converted back into DC power at the receiver side. This method is increasingly popular in the fields of wireless sensor networks and remote power supply systems, especially where traditional wired options are impractical or unreliable [1], [2].

A key element in the RF-WPT transmitter is the RF power amplifier (PA), which heavily influences overall system efficiency, output power, and thermal management. When the PA operates inefficiently, it causes significant energy waste, shorter transmission distances, and reliability issues, especially in high-power WPT scenarios. Therefore, an efficient high-power PA design is crucial to support reliable and sustained wireless energy delivery [1], [2].

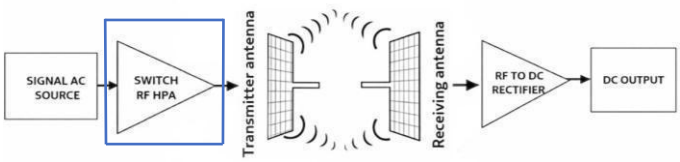


Figure 1: Wireless Power Transfer Block Flow Using RF HPA Technology

Class-E power amplifiers are known for their efficient switching behavior, thanks to the soft switching mechanism that reduces losses during the switching process. Theoretically, these amplifiers can achieve efficiencies above 80%, making them a strong choice for RF-WPT transmitters. However, the power output of a single Class-E amplifier is naturally limited by the device's voltage limits, current capacity, and thermal tolerance [2].

To overcome this limitation, a parallel Class-E power amplifier configuration has been introduced, where several amplifier modules work together and share the RF load. The signals are combined through a hybrid coupler, offering minimal signal loss, balanced amplitude and phase, as well as inherent isolation between the amplifier paths. This

configuration increases total power while maintaining high efficiency and reducing both electrical and thermal stress on each component, making it ideal for high-power RF-WPT applications that demand maximum performance [1], [2].

In RF power amplifier design for WPT, a parallel architecture is selected over a cascaded configuration because the primary objective is to maximize power handling capacity and thermal distribution rather than merely increasing the small-signal gain. A cascaded topology connects amplifier stages sequentially to boost gain, which creates a bottleneck at the final stage that must handle the entire thermal and electrical load, thereby limiting the maximum output power. Conversely, the parallel topology splits the RF load equally across multiple GaN HEMT modules. This approach allows the system to achieve a substantially higher total output power while maintaining soft-switching high efficiency and preventing early device breakdown [10], [11], [13].

The incorporation of Gallium Nitride High Electron Mobility Transistor (GaN HEMT) technology further enhances the potential for robust and efficient RF power amplifiers. GaN HEMT devices provide strong breakdown voltage capabilities, high current flow, and superior thermal management, allowing them to function at higher voltages and power outputs. Therefore, the combination of parallel Class-E designs, hybrid coupler-based signal combining, and GaN HEMT technology forms a solid foundation for advanced high-power wireless power transfer transmitters [1], [2].

The choice of 2.6 GHz operating frequency is based on balancing the optimal trade-off between the physical size of the device and the efficiency of electromagnetic wave propagation [4], [17]. At this microwave frequency range, the dimensions of the matching network and the transmitting/receiving antenna components can be designed more compactly, making it ideal for portable WPT applications like integration into Unmanned Aerial Vehicles (UAVs) [1]. Moreover, the 2.6 GHz frequency has a propagation path loss that is still tolerable, ensuring that high-power wireless energy transmission can be carried out efficiently over medium distances [3], [6].

Beyond theoretical studies, wireless power transfer (WPT) technology plays a critical role in various practical applications that require long-distance electrical energy transmission without physical connections. A primary application of high-power WPT is in medium- to high-power wireless charging systems, such as power supplies for remote sensors, environmental monitoring systems, unmanned aerial vehicles (UAVs), and large-scale wireless electric vehicle (EV) charging platforms [1], [3], [4], [6]. In these heavy-duty applications, conventional wired charging becomes inefficient, poses severe electrical safety risks, or is physically unfeasible due to dynamic movement and high energy demands. Consequently, advanced high-power RF transmitter systems equipped with efficient high-power amplifiers (HPAs) are strictly required to ensure that substantial amounts of energy can be transmitted reliably, safely, and sustainably to electric vehicles and remote operational platforms [1], [3], [6].

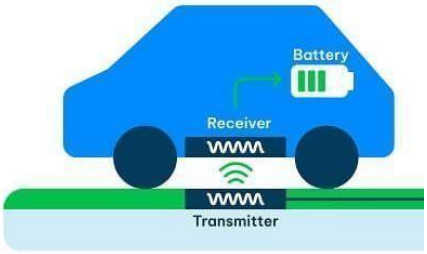


Figure 2: Illustration of Wireless Power Transfer (WPT) for Electric Vehicle Battery Charging.

II. THEORETICAL BACKGROUND

A. High Power Amplifier (HPA)

High-Power RF Amplifiers (HPA) are key components in RF transmitters for Wireless Power Transfer (WPT), as they are responsible for converting DC energy into high-power RF signals. The performance of an HPA directly affects the transfer range, efficiency, and the quality of power received by the WPT system. Important HPA parameters include input power, output power, drain efficiency, Power Added Efficiency (PAE), gain, and DC power consumption. Theoretical analysis at this stage is crucial to establish the operating limits of GaN-HEMT transistors, which serve as the main amplifiers in the design of parallel Class-E amplifiers [5].

Based on various studies on RF amplifiers, it has been revealed that the choice of topology and matching method greatly determines amplifier performance. For WPT applications, the amplifier needs to operate in a high efficiency mode with minimal power loss, making switching modes like Class-E more suitable. In addition, the advantages of GaN-HEMT transistors including high breakdown voltage, high electron mobility, and the ability to operate at high frequencies make this topology a primary choice. Mathematical analysis of HPA power parameters is required to ensure the design meets the specified output power and efficiency requirements [6].

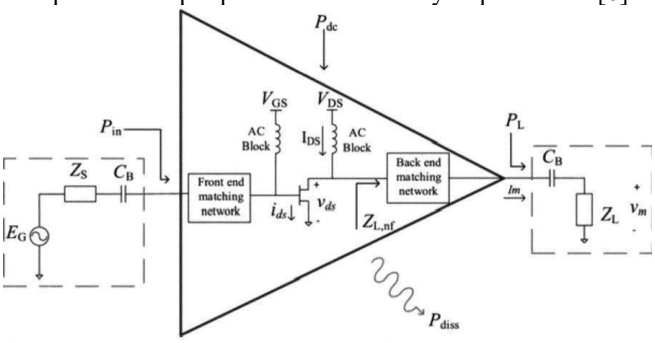


Figure 3: High Power Amplifier Schematic General

The power input to the HPA is the power of the signal at the amplifier's input terminal:

$$P_{in} = V_{in} . I_{in}$$

Where:

V_{in} : Voltage at the input (V)

I_{in} : Current at the input (A)

The power output of the amplifier is the power of the amplified signal delivered at the output terminal:

$$P_{out} = V_{out} . I_{out}$$

Where:

V_{out} : Voltage at the output (V)
I_{out} : Current at the output (A)

The total DC power consumed by the HPA, derived from the supply voltage and current:

$$P_{DC} = V_{B1} . I_{B1} + V_{B2} . I_{B2}$$

Where:

B_1 : Bias network gate
B_2 : Bias network drain

Delivered power is the power effectively transmitted to the load:

$$P_{delivered} = \frac{V^2_{out}}{R_{load}}$$

Where:

V_{out} : Output voltage (V)
R_{load} : Load resistance (Ohm)

Efficiency measures how effectively the amplifier converts DC input power into RF output power:

$$\eta = \frac{P_{out}}{P_{DC}}$$

Power Added Efficiency (PAE) quantifies how efficiently an amplifier converts the additional DC power into an amplified RF signal, considering the gain:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out} - P_{gain}}{P_{DC}} = \eta \left(1 - \frac{1}{P_{gain}}\right)$$

Power gain (dBm) is defined as a range of output power to input power:

$$P_{gain} = P_{out} - P_{in}$$

B. Class E

The Class E implementation with transmission line can be defined as an amplifier with an active device operating as an ideal switch and load network which there is no voltage drop across the switch when the switch is on. The switch has zero resistance when it is turned on and infinite resistance when it is off [2], [8].

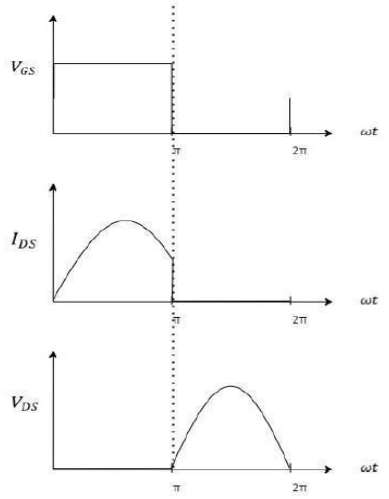


Figure 4: Voltage and Current Waveforms the Ideal Class-E

To implement the class E topology, a short circuit stub with a value of λ/8 is given along with an open circuit stub λ/8. These two stubs function to impose a short circuit termination (Zin = ∞) on the second harmonic frequency and an open circuit termination (Zin = 0) on the first and third harmonic frequencies. The series with a value of λ/6 and the stub with a value of λ/12 are open circuits that function to enforce short-circuit termination at the third harmonic frequency and as the output matching network

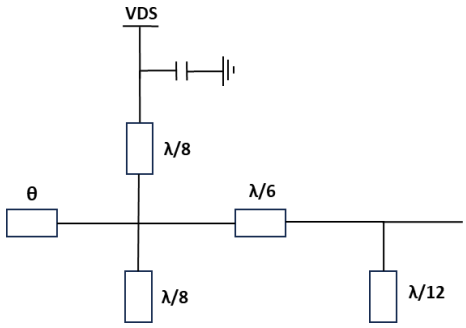


Figure 5: Class E Implementation with Transmission Line

C. Hybrid Coupler

A hybrid coupler is a four-port network that divides and combines RF power in a balanced manner with a specific phase difference and good isolation between ports, making it ideal for use as a power combiner in parallel Class-E power amplifiers for wireless power transfer systems [13].

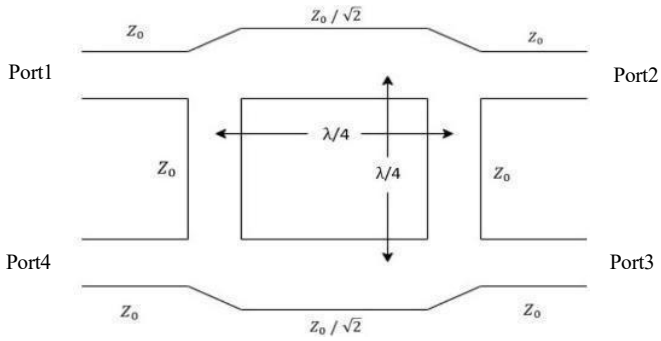


Figure 6: Design Approaches for Hybrid Coupler.

As illustrated in the hybrid coupler structure, two different characteristic impedances are employed to achieve equal power division and proper impedance matching [14], [15].

The horizontal transmission lines have an impedance of:

$$Z_1 = \frac{Z_0}{\sqrt{2}}$$

while the vertical branch lines have an impedance of:

$$Z_2 = Z_0$$

where Z_0 is the system characteristic impedance, typically 50 Ω.

This impedance ratio ensures that the input power is equally divided between the output ports (−3 dB), maintains impedance matching at all ports, and provides isolation between the output branches [14].

An ideal branch-line hybrid coupler satisfies the following S-parameter conditions:

- Ideal S-Parameter Characteristics:

$$|S_{21}| = |S_{31}| = \frac{1}{\sqrt{2}}$$

- Quadrature Phase Difference:

$$\angle S_{21} - \angle S_{31} = 90°$$

- Input Matching:

$$S_{11} = 0$$

- Isolation Between Output Ports:

$$S_{23} = 0$$

In a parallel Class-E amplifier configuration, these conditions ensure that both amplifier branches receive equal excitation, remain electrically isolated from each other, and maintain stable operation even under minor load mismatches [13].

III. RESEARCH METHODOLOGY

Figure 1 below shows the the block diagram for designed High Power Amplifier. The power input of the circuit is Pin = 31 dBm and the frequency is 2.6 GHz.

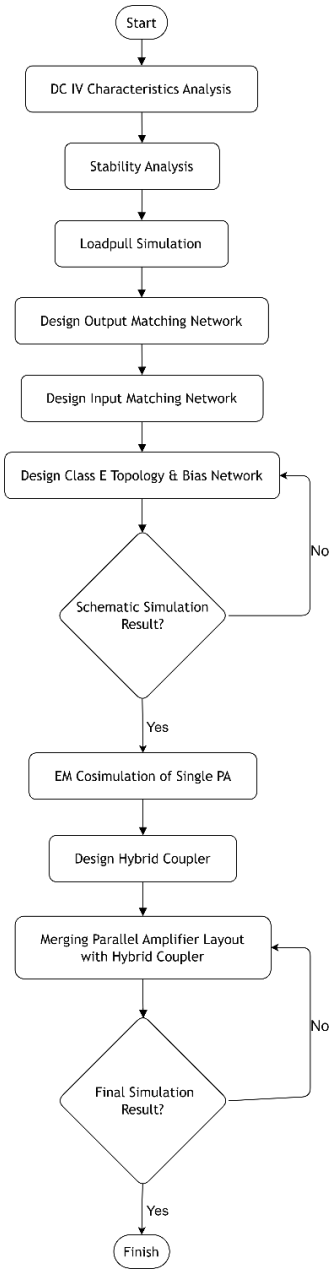


Figure 7: The Block Diagram for Designed High Power Amplifier Class-E

The design methodology, as illustrated in the block diagram, is structured to systematically build and validate the high-power amplifier. The process begins with DC IV Characteristics Analysis to determine the optimal active biasing point for Class-E operation, followed by Stability Analysis to ensure the GaN transistor remains unconditionally stable without unwanted high-frequency oscillations. A Loadpull Simulation is then executed to precisely extract the optimum source (Z_S_opt) and load (Z_L_opt) impedances required to maximize both Power Added Efficiency (PAE) and output power. These extracted values drive the Design of Input and Output Matching Networks, which utilize specific transmission line geometries to eliminate signal reflections. Subsequently, the Class-E Topology and Bias Network are integrated and initially validated through a schematic Harmonic Balance

simulation. To accurately account for physical PCB parasitic effects, an EM Co-simulation is performed on the microstrip layout. Finally, the Hybrid Coupler is independently designed to divide and combine power evenly, culminating in the Merging of the Parallel Amplifier Layout, where the complete balanced architecture is simulated to verify the absolute final power delivery performance.

A. Simulation of DC IV Characteristics

DC IV Characteristics is the first process to design a High Power Amplifier. This simulation aims to determine the working point of the High Power Amplifier class E by providing drain bias and gate bias on the GaN HEMT transistor GTVA2627011 from supplier Macom Wolfspeed. For a schematic diagram, can be seen from the figure 8.

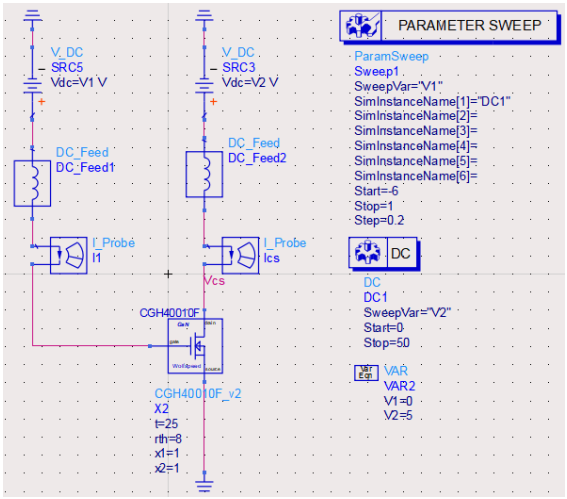


Figure 8: DC IV Characteristics Schematic

When the transistor is given a bias of 28V on the drain and -2.7V on the gate, the working point is selected at the condition where the current flowing in the transistor is close to 0A (4.132E-5 A) and the voltage is 28V. The simulation results at this stage show that the transistor is able to provide a maximum RF power output of 11.522 W with an efficiency of 77.138 %. The flowing IDC current is 0.63 A, the conduction angle is 187.83 degrees, and the duty cycle is 52.17%, as shown in the figure below. However, it is important to note that these DC IV loadline simulation results indicate a Class A operation (360-degree conduction angle).

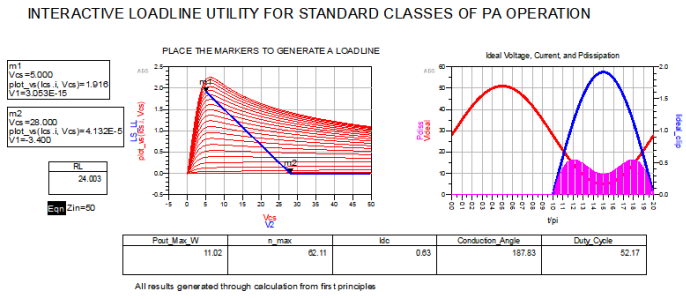


Figure 9: DC IV Characteristics Result

B. Simulation of Stability Analysis

This is the second process that aims to analyze the stability and transistors used whether they are unconditionally stable or conditionally unstable. In the schematic configuration, several essential discrete components are integrated to ensure proper DC biasing and high-frequency signal integrity. DC voltage sources and bias VDC are utilized to provide the required operating voltages, such as drain and gate biases, to establish the correct DC operating point for the GaN HEMT transistor. Furthermore, *RF chokes* or *DC feeds* act as high-impedance elements on the bias lines, allowing DC current to flow into the transistor while preventing high-frequency RF signals from leaking into the power supply. *DC blocking* capacitors are placed in series along the main signal path to separate the direct current component from high-frequency alternating signals, thereby preventing high DC voltages from reaching external ports or measuring equipment while ensuring that only RF signals are transmitted with minimal resistance. Additionally, terminals (*Term G*) with standard characteristic impedance are used as port terminations to define signal inputs/outputs and perform S-parameter measurements during simulation.

A transistor is said to be absolutely stable if the stability factor (K)>1 and the magnitude delta (mag_delta) < 1. Similarly, it is said to be unstable if the stability factor (K)<1 and the magnitude of delta (mag_delta) are > 1. For the sematic network can be seen in the figure below:

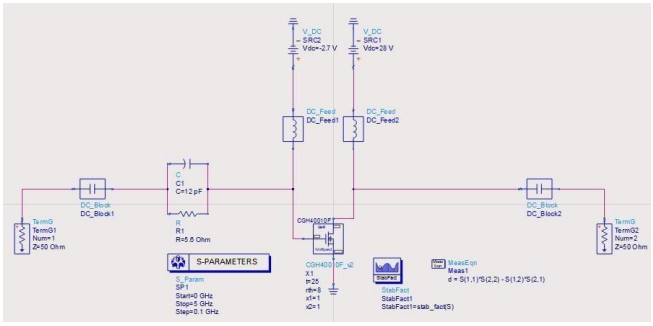


Figure 10: Stability Analysis Schematic

The simulation results stated that at the working frequency of 2.6 GHz, the stability factor value (K) >1 was **1.501** and the magnitude value (mag_delta) <1 was **0.259** so that the GaN HEMT transistor CGH40010F was in an unconditionally stable condition and the S-parameter table results can be seen in the figure below:

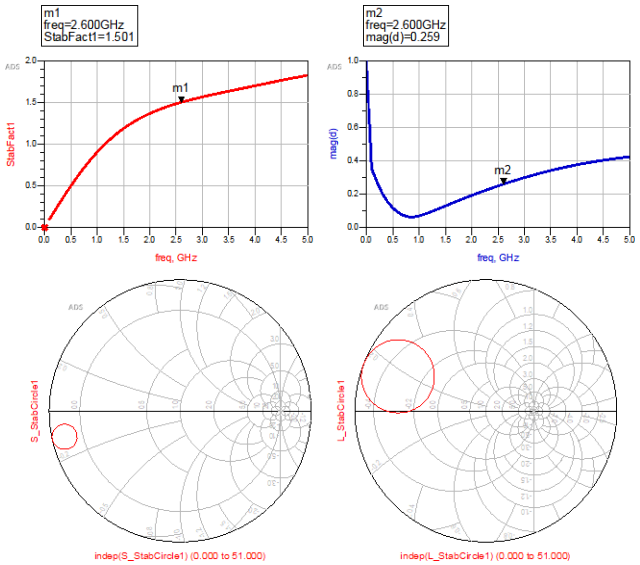


Figure 11: Stability Analysis Result

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
2.600 GHz	0.820 / 167.453	0.021 / -34.214	3.634 / 42.788	0.409 / -158.409

Figure 12: S-parameter Table Result

C. Simulation of Loadpull

Loadpull is a simulation used to determine how much RF power input value should be given to the transistor, the optimal load impedance value at the transistor drain (ZL opt) and the optimal source impedance value at the transistor gate (ZS opt), in order to obtain high Power Added Efficiency (PAE) (above 60%), high gain (above 10 dB) and high RF power output (above 41.486 dBm). The loadpull schematic using the loadpull instrument and its parameters is in accordance with the schematic in the figure below:

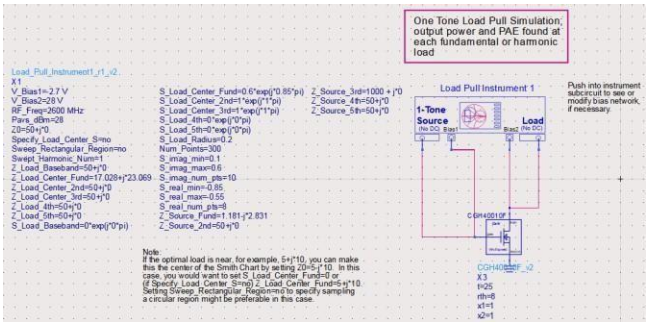


Figure 13: Loadpull Schematic

When the RF power input value is given to the transistor of 28 dBm, ZL opt is 17.062 + j14.004 and Zin is 1.300 + j0.675 where under this condition, PAE is achieved 67.893%, gain of 13.486 dB (amplifier) and RF power output = 41.486 dBm. The results of the simulation can be seen from the two figures below:

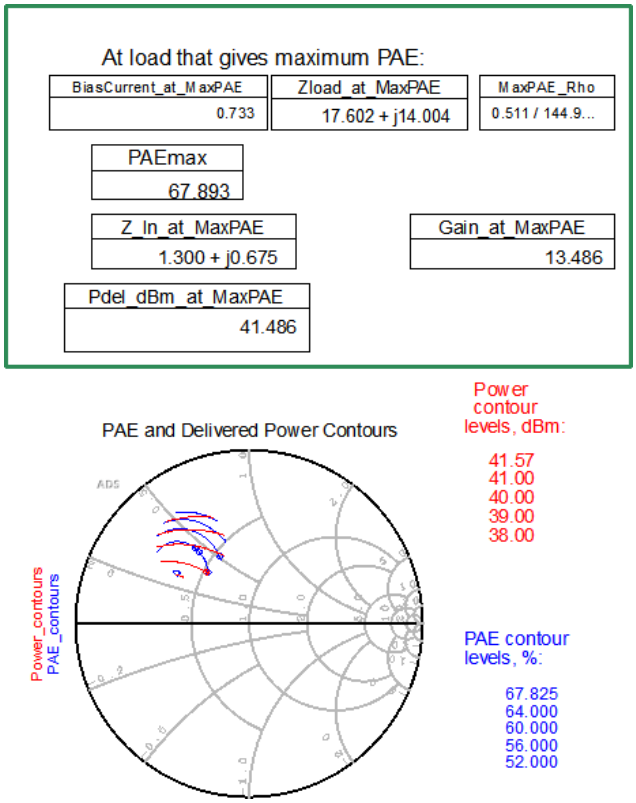


Figure 14: Loadpull Result

D. Design of Output Matching Network

In the design of high-power RF amplifiers, particularly for highly non-linear switching modes like Class-E, standard small-signal matching techniques based on traditional S-parameters cannot be used to determine the optimum termination impedances. Under large-signal excitation, the GaN HEMT transistor's internal capacitances, resistances, and transconductance vary significantly with the high input power level, rendering small-signal linear assumptions invalid. Therefore, the impedance matching targets must be derived from a large-signal Load-Pull simulation. The Load-Pull method empirically sweeps various impedances at the actual high-power operating point to find the exact large-signal source (Z_in) and load (Z_L_opt) impedances required to achieve the maximum Power Added Efficiency (PAE) and output power. Consequently, these specific large-signal impedances are extracted directly from the maximum PAE contours and used as the absolute reference targets for synthesizing the matching networks, bypassing the traditional small-signal conjugate matching process.

After obtaining the ZL opt parameter from the loadpull result, the next step is to design the output matching network impedance matching between the ZL opt = 17.602 + j*14.004 and the 50 Ohm output ZL. This aims to make the S22 parameter that the output return loss has the smallest possible reflection (gamma) close to 0 and in the minimum possible dB (S22<-20 dB), To implement this Output Matching Network, a cross-junction Cros2 is installed as the main path alongside transmission line segments MLIN (TL8). This circuit is equipped with MLOC stubs (TL32) that function as reactive

elements to fine-tune the output impedance and ensure optimal termination at the 50-ohm load, achieving maximum output power efficiency. The schematic of the network can be seen in the figure below:

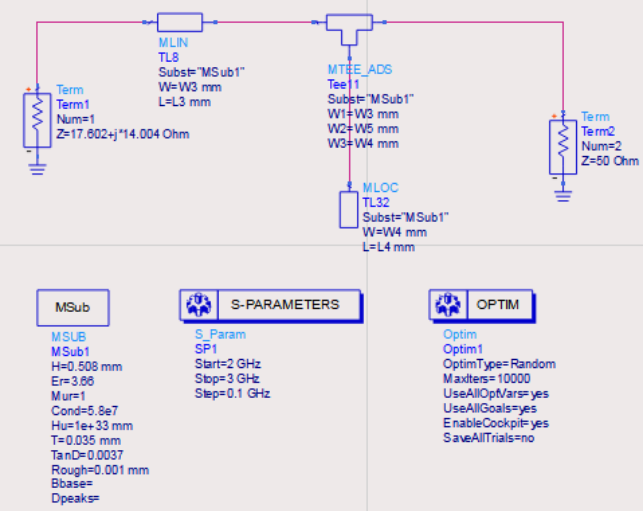


Figure 12: Output Matching Network Schematic

The simulation results showed that the S22 parameter was valued at -46.267 dB at a frequency of 2.6 GHz and corresponded to the desired specification (S22 <-20dB). Similarly, when S22 is plotted in the smith chart, the normalized impedance value is in the position of 0.992 + j0.006 (close to the center point of smith chart = 1) and the gamma value S22 = 0.005 (close to 0) so that the impedance condition is matched. The two simulation results can be seen in the figure below:

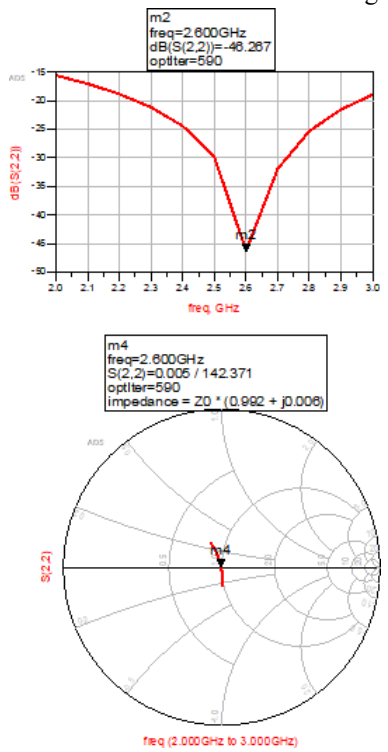


Figure 13: Output Matching Network Result

E. Design of Input Matching Network

After obtaining the ZS opt parameter from the loadpull result, the next step is to design the input matching network impedance matching between the ZS = 50 Ohm and ZS opt = 1.300 + j0.676. This aims to make the S11 parameter that the output return loss has the smallest possible reflection (gamma) close to 0 and in the minimum possible dB (S11<-20 dB), So that the RF input power can be transmitted optimally to the transistor, the main transmission path is formed using MLIN elements (TL30) integrated via MTEE_ADS junctions (Tee9). Using a single open stub and a single transmission line, the MLOC stub (TL28) functions as a reactive element to transform the source impedance into the input impedance required by the HEMT transistor gate, in order to minimize reflection losses and ensure efficient conjugate matching at the operating frequency. The schematic of the network can be seen in the figure below:

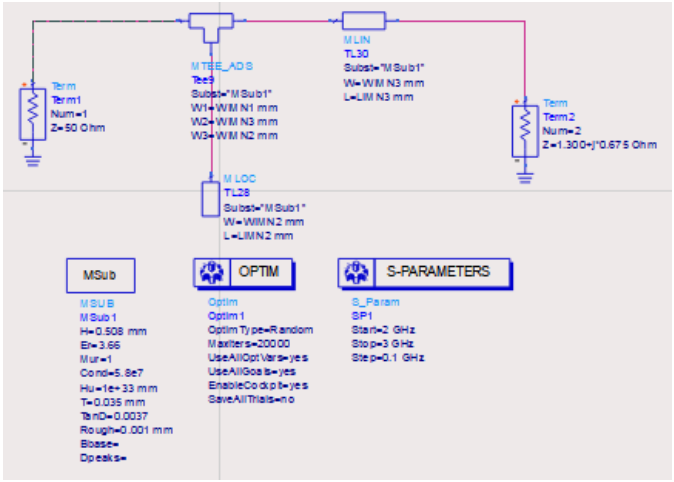


Figure 14: Input Matching Network Schematic

The simulation results showed that the S11 parameter was valued at -50.402 dB at a frequency of 2.6 GHz and corresponded to the desired specification (S11 <-20dB). Similarly, when S11 is plotted in the smith chart, the normalized impedance value is in the position of 1.004 + j0.004 (close to the center point of smith chart = 1) and the gamma value S11 = 0.003 (close to 0) so that the impedance condition is matched. The two simulation results can be seen in the figure below:

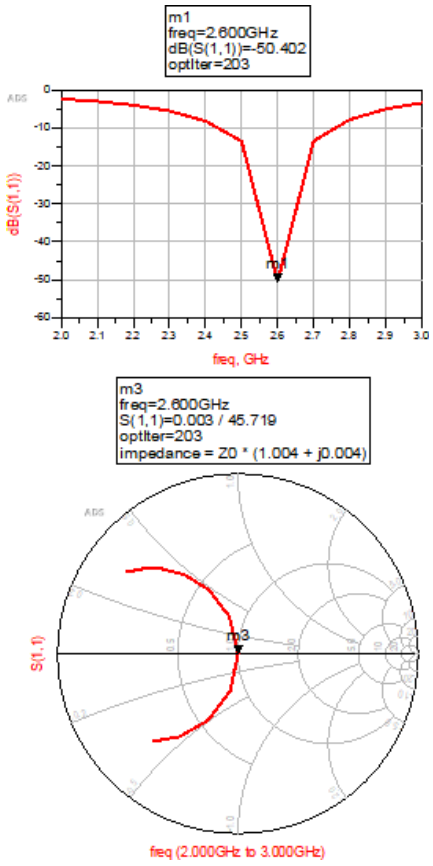


Figure 15: Input Matching Network Result

F. Design of Class-E Topology

The figure below presents the full schematic of the entire Class E power amplifier design. This integrated circuit combines all previously designed subsystems. In addition to routing and shaping the RF signals, this schematic integrates the DC biasing system without disrupting high-frequency performance. I also designed the bias networks on the gate and drain sides using a combination of a quarter-wavelength (λ/4) transmission line and a microstrip radial stub (MRSTUB). The λ/4 transmission line acts as an impedance transformer to connect the main RF path to a virtual short-circuit point on the MRSTUB, with a physical length (l) calculated based on the 2.6 GHz operating frequency and the effective dielectric constant (ε_eff) of the Rogers RO4350B substrate.

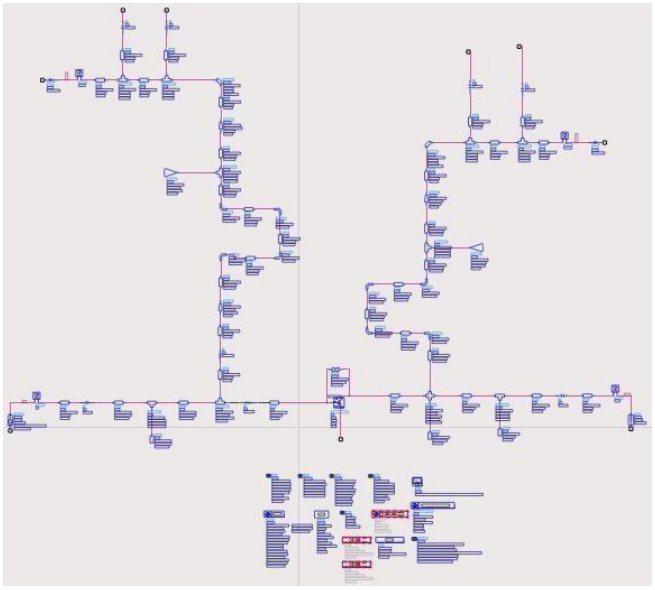
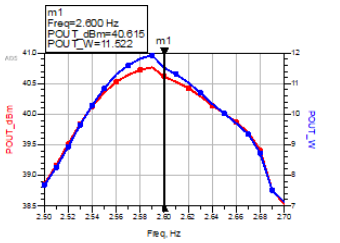


Figure 19: Full Schematic Class E Topology

A Harmonic Balance simulation was then performed on the full schematic at a frequency of 2.6 GHz. The simulation results for Pout, Pgain, DE, and PAE can be seen in Figure 19 below. Based on the schematic simulation, the Class-E parallel GaN HEMT amplifier demonstrates high performance. The amplifier yields a massive output power (Pout) of 40.615 dBm (approximately 11.522 W). The small-signal gain (S21) reaches 21.632 dB, with an excellent return loss (S11) of -23.213 dB. Furthermore, the achieved Power Added Efficiency (PAE) was 74.641 %, and the Drain Efficiency (DE) was 77.138%.

Freq	PIN_dBm	PIN_W	POUT_dBm	PDC_W	POUT_dBm	GAIN_dB	PAE	EFFICIENCY	PDC_W
2.500 Hz	20.060	0.101	38.853	14.151	38.853	10.853	53.544	54.261	14.151
2.510 Hz	20.459	0.111	39.167	14.576	39.167	11.167	55.868	56.630	14.576
2.520 Hz	20.879	0.122	39.515	15.015	39.515	11.515	58.743	59.558	15.015
2.530 Hz	21.357	0.137	39.847	15.350	39.847	11.847	62.007	62.897	15.350
2.540 Hz	21.910	0.155	40.128	15.554	40.128	12.128	65.220	66.219	15.554
2.550 Hz	22.524	0.179	40.355	15.656	40.355	12.355	68.164	69.307	15.656
2.560 Hz	23.194	0.209	40.532	15.626	40.532	12.532	71.010	72.345	15.626
2.570 Hz	23.885	0.245	40.644	15.495	40.644	12.644	73.280	74.859	15.495
2.580 Hz	24.582	0.287	40.729	15.366	40.729	12.729	75.101	76.970	15.366
2.590 Hz	25.250	0.336	40.767	15.269	40.767	12.767	76.007	78.202	15.269
2.600 Hz	25.777	0.378	40.615	14.937	40.615	12.615	74.606	77.138	14.937
2.610 Hz	26.370	0.434	40.531	14.906	40.531	12.531	72.901	75.810	14.906
2.620 Hz	26.961	0.497	40.429	14.332	40.429	12.429	73.557	77.022	14.332
2.630 Hz	27.404	0.550	40.296	13.953	40.296	12.296	72.776	76.718	13.953
2.640 Hz	27.715	0.591	40.144	13.757	40.144	12.144	70.850	75.145	13.757
2.650 Hz	27.831	0.607	40.013	13.260	40.013	12.013	71.064	75.641	13.260
2.660 Hz	27.739	0.594	39.869	13.197	39.869	11.869	69.016	73.518	13.197
2.670 Hz	27.318	0.539	39.708	13.086	39.708	11.708	67.325	71.446	13.086
2.680 Hz	26.659	0.463	39.406	13.533	39.406	11.406	61.029	64.453	13.533
2.690 Hz	25.583	0.362	38.758	13.224	38.758	10.758	54.081	56.815	13.224
2.700 Hz	24.090	0.256	38.524	12.031	38.524	10.524	57.043	59.175	12.031



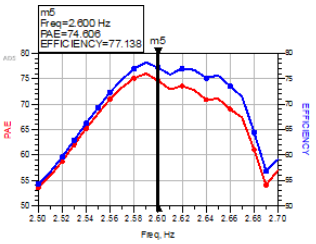


Figure 19: Full Schematic Class E Topology Result

To ensure that the RF HPA works in class E topology, the voltage and current waveforms on the intrinsic transistor are plotted. It can be seen that when the voltage is off (0V), the current flows (1.7A). Meanwhile, when the voltage is on (78V), the current does not flow (0A).

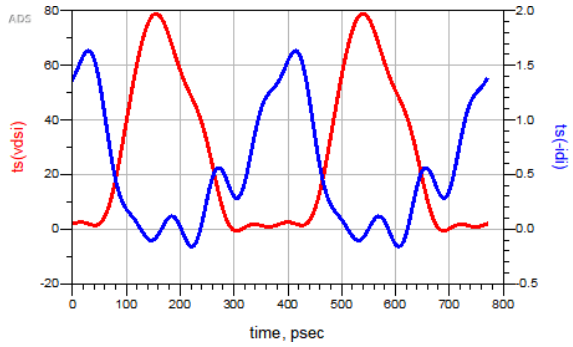


Figure 20: Voltage and Current Waveform at Intrinsic Device Node

Since the initial schematic simulation results have been achieved successfully, then convert the layout according to the PCB parameters of the Rogers Duroid 4350.

G. Simulation of EM Cosimulation

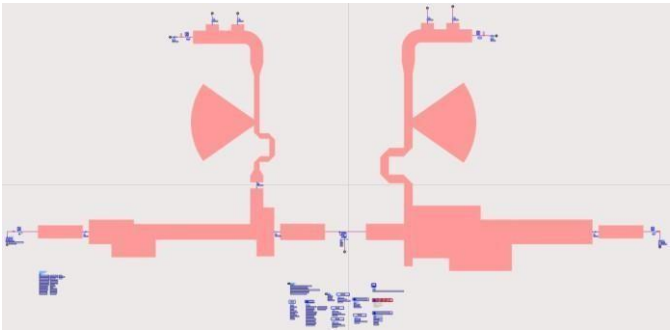


Figure 21: Single PA EM Cosimulation Schematic

After successfully achieving the initial schematic simulation results, the layout is converted according to the physical PCB parameters for a Single PA to analyze the electromagnetic behavior. The EM co-simulation of the single GaN HEMT Class E RF High Power Amplifier yields the Pout, Pgain, DE, and PAE values as shown in the figure 22 below. The results show a shift in performance due to the parasitic effects of the physical layout traces. At the 2.6 GHz frequency, the single PA delivers a Pout of 39.067 dBm (8.066 W). The small-signal gain (S21) is 15.081 dB with a return loss (S11) of -19.780 dB. The efficiency parameters achieved are 66.266 % for PAE and 71.749 % for DE. This indicates that the single PA operates efficiently, although the physical layout introduces minor degradations compared to the ideal schematic.

Freq	PIN_dBm	PIN_W	POUT_dBm	PDC_W	POUT_dBm	GAIN_dB	PAE	EFFICIENCY	PDC_W
2.500 Hz	26.945	0.495	39.405	13.014	39.405	11.405	63.194	66.997	13.014
2.510 Hz	27.071	0.509	39.391	12.906	39.391	11.391	63.397	67.344	12.906
2.520 Hz	27.191	0.524	39.373	12.787	39.373	11.373	63.587	67.683	12.787
2.530 Hz	27.307	0.538	39.352	12.663	39.352	11.352	63.784	68.032	12.663
2.540 Hz	27.415	0.551	39.330	12.529	39.330	11.330	64.000	68.401	12.529
2.550 Hz	27.518	0.565	39.303	12.371	39.303	11.303	64.281	68.846	12.371
2.560 Hz	27.613	0.577	39.271	12.187	39.271	11.271	64.632	69.367	12.187
2.570 Hz	27.699	0.589	39.232	11.979	39.232	11.232	65.040	69.955	11.979
2.580 Hz	27.777	0.599	39.187	11.747	39.187	11.187	65.493	70.595	11.747
2.590 Hz	27.843	0.608	39.134	11.493	39.134	11.134	65.987	71.283	11.493
2.600 Hz	27.899	0.616	39.067	11.242	39.067	11.067	66.266	71.749	11.242
2.610 Hz	27.942	0.623	38.978	11.029	38.978	10.978	66.017	71.662	11.029
2.620 Hz	27.973	0.627	38.884	10.824	38.884	10.884	65.669	71.462	10.824
2.630 Hz	27.989	0.629	38.793	10.634	38.793	10.793	65.307	71.225	10.634
2.640 Hz	27.991	0.630	38.703	10.446	38.703	10.703	64.998	71.025	10.446
2.650 Hz	27.978	0.628	38.612	10.243	38.612	10.612	64.795	70.923	10.243
2.660 Hz	27.949	0.624	38.520	10.029	38.520	10.520	64.696	70.913	10.029
2.670 Hz	27.904	0.617	38.426	9.802	38.426	10.426	64.701	70.998	9.802
2.680 Hz	27.844	0.609	38.326	9.558	38.326	10.326	64.791	71.160	9.558
2.690 Hz	27.768	0.598	38.206	9.345	38.206	10.206	64.398	70.798	9.345
2.700 Hz	27.677	0.586	38.072	9.146	38.072	10.072	63.744	70.149	9.146

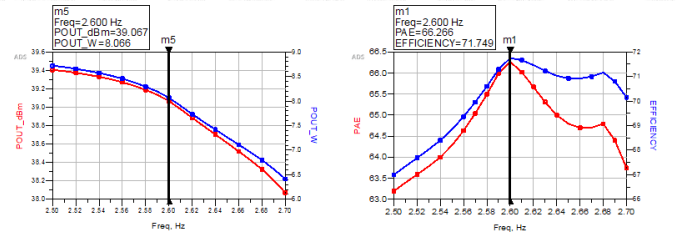


Figure 22: Single PA EM Cosimulation Result

Likewise, to ensure that the RF HPA works in class E topology, the voltage and current waveforms on the intrinsic transistor are plotted. The waveform condition is still in class E topology, but there is a decrease in the Vmax value to 75V and a decrease in Imax to 1.1A. This condition is still stable and suitable for class E topology.

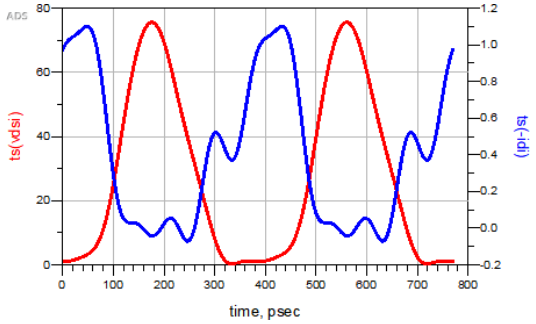


Figure 23: Voltage and Current Waveform at Intrinsic Device Node

H. Design Hybrid Coupler

To divide the input power equally and provide a 90-degree phase shift for the parallel Class E amplifier, a hybrid coupler is designed and optimized at the operating frequency of 2.6 GHz. The design utilizes a microstrip transmission line topology, and an optimization process is performed to achieve the best S-parameter values and phase difference. The schematic of the designed hybrid coupler can be seen in the figure below:

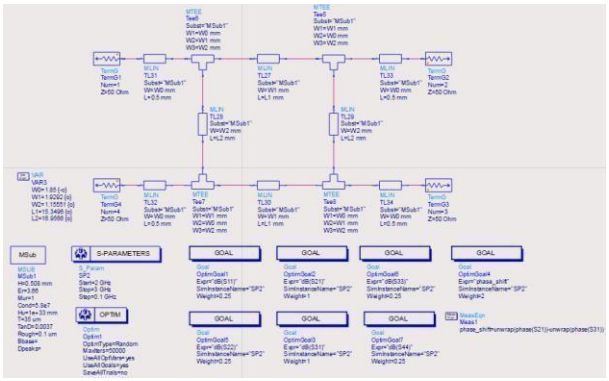


Figure 24: Hybrid Coupler Schematic

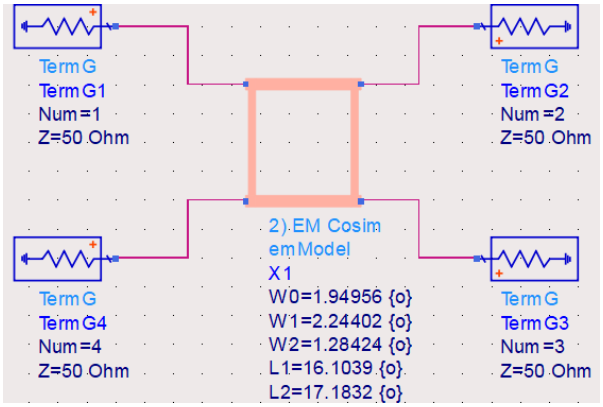


Figure 25: Hybrid Coupler Layout

The simulation results demonstrate excellent performance of the hybrid coupler at 2.6 GHz. The return loss (S11) is achieved at -41.586 dB, and the isolation (S41) is -33.290 dB, indicating minimal reflection and excellent port isolation. The power is split almost equally, with the through port (S21) at -3.115 dB and the coupled port (S31) at -3.176 dB. Furthermore, the phase difference between the two output ports is 89.972 degrees, which perfectly meets the strict requirement of a 90-degree hybrid coupler. The simulation results are shown in the figure below:

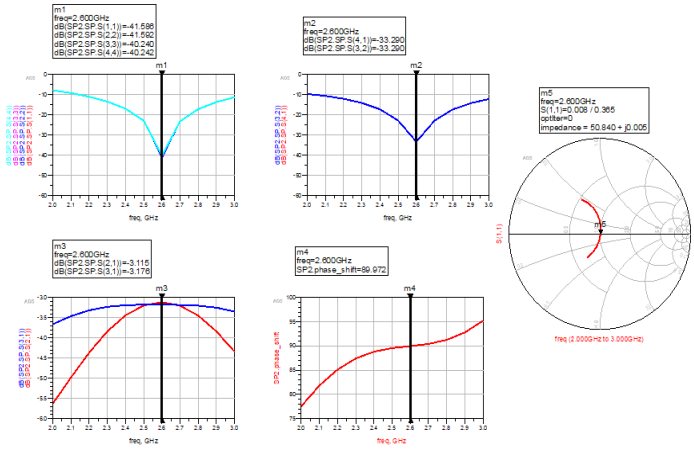


Figure 26: Hybrid Coupler Network Result

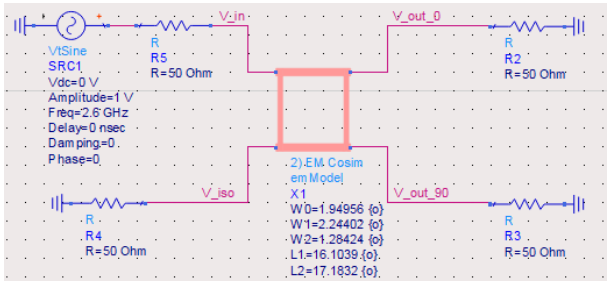


Figure 27: Transient Simulation Test Circuit of the Hybrid Coupler.

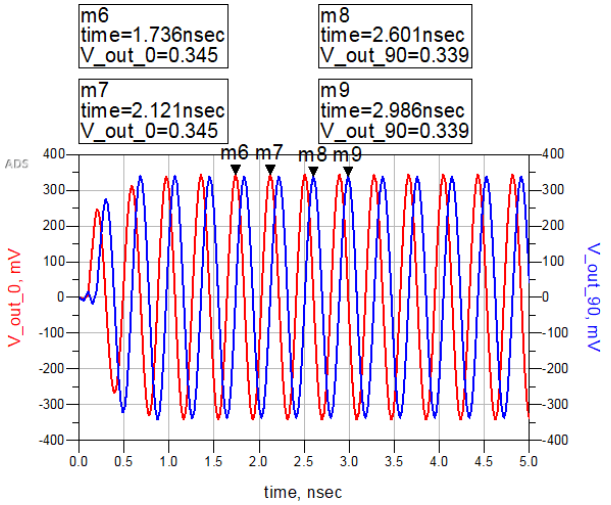


Figure 28: Time-Domain Transient Simulation Waveforms

First, frequency validation on the primary (Thru) path. Using markers m6 (1.736 ns) and m7 (2.121 ns) on the red wave, the time difference is precisely 385 picoseconds. This accurately represents one full period at our target frequency of 2.6 GHz. Second, signal integrity on the coupled path. Markers m8 (2.601 ns) and m9 (2.986 ns) on the blue wave yield the exact same time difference of 385 picoseconds. This proves that the 90-degree diverted signal suffers no frequency distortion and maintains perfect operation at 2.6 GHz. Third, the equal power split and phase shift. The red wave achieves a peak amplitude of 345 mV, while the blue wave sits at 339 mV. This nearly identical amplitude confirms a balanced -3 dB power division. The negligible 6 mV deviation is a highly realistic outcome attributed to physical insertion losses captured during the EM Co-simulation. Furthermore, observing the peak-to-peak distance, the blue wave is consistently delayed by exactly one-quarter of a cycle relative to the red wave. This definitively validates the 90-degree quadrature phase shift, an absolute prerequisite for this parallel amplifier architecture.

I. Merging the Parallel Amplifier Layout with Hybrid Coupler

After the EM co-simulation results for the single PA were verified, the process continued by integrating two identical Single PA layouts with the previously designed hybrid couplers at both the input and output stages. The final layout of the balanced parallel amplifier, including the ground-via holes and

the DC bias routing lines, is presented in Figure 29. The final dimension of the compact parallel amplifier is 155.874 mm × 93.083 mm.

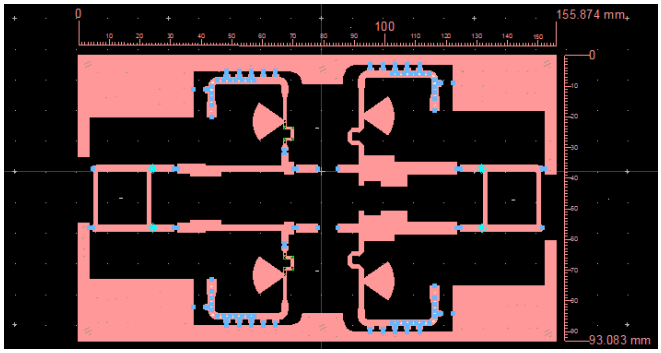


Figure 29: Final Layout Parallel with the Hybrid Coupler

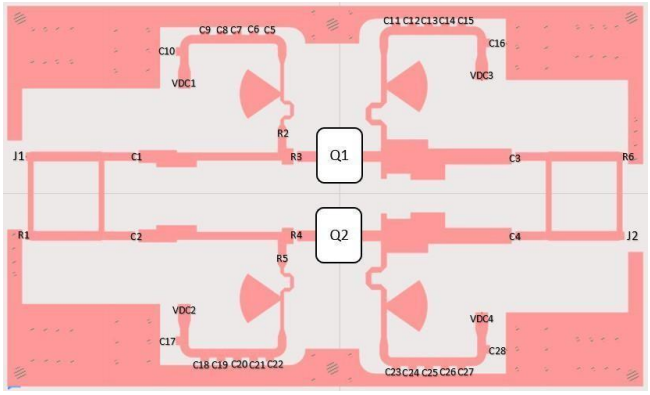


Figure 30: PCB Component Placement Diagram

To ensure stability and proper DC biasing, discrete components are placed strategically across the layout. As shown in Figure 30, bypass capacitors (varying from 0.5 pF to 56 µF) are routed on the DC supply lines to filter out RF leakages and maintain bias stability. Isolation resistors (50 Ohms) are placed at the isolated ports of the hybrid couplers to absorb any reflected or unbalanced power.

Freq	PIN_dBm	PIN_W	POUT_dBm	PDC_W	POUT_dBm	GAIN_dB	PAE	EFFICIENCY	PDC_W
2.500 Hz	30.935	1.240	42.735	14.672	42.735	11.735	59.748	63.974	14.672
2.510 Hz	30.948	1.244	42.790	14.772	42.790	11.790	60.135	64.345	14.772
2.520 Hz	30.959	1.247	42.825	14.770	42.825	11.825	60.650	64.872	14.770
2.530 Hz	30.969	1.250	42.839	14.655	42.839	11.839	61.332	65.597	14.655
2.540 Hz	30.978	1.253	42.833	14.435	42.833	11.833	62.166	66.504	14.435
2.550 Hz	30.985	1.254	42.799	14.210	42.799	11.799	62.624	67.038	14.210
2.560 Hz	30.990	1.256	42.746	14.064	42.746	11.746	62.440	66.906	14.064
2.570 Hz	30.994	1.257	42.672	13.860	42.672	11.672	62.203	66.738	13.860
2.580 Hz	30.997	1.258	42.588	13.564	42.588	11.588	62.250	66.887	13.564
2.590 Hz	30.999	1.259	42.503	13.179	42.503	11.503	62.729	67.504	13.179
2.600 Hz	30.999	1.259	42.410	12.693	42.410	11.410	63.658	68.617	12.693
2.610 Hz	30.999	1.259	42.292	12.173	42.292	11.292	64.453	69.623	12.173
2.620 Hz	30.999	1.259	42.161	11.858	42.161	11.161	64.044	69.350	11.858
2.630 Hz	30.998	1.258	42.007	11.560	42.007	11.007	63.221	68.663	11.560
2.640 Hz	30.996	1.258	41.874	11.172	41.874	10.874	63.269	68.898	11.172
2.650 Hz	30.994	1.257	41.733	10.669	41.733	10.733	63.954	69.845	10.669
2.660 Hz	30.990	1.256	41.567	10.201	41.567	10.567	64.152	70.309	10.201
2.670 Hz	30.985	1.254	41.406	9.957	41.406	10.406	63.123	69.423	9.957
2.680 Hz	30.977	1.252	41.244	9.731	41.244	10.244	61.986	68.421	9.731
2.690 Hz	30.970	1.250	41.102	9.432	41.102	10.102	61.703	68.330	9.432
2.700 Hz	30.960	1.247	40.928	9.040	40.928	9.928	61.593	68.493	9.040

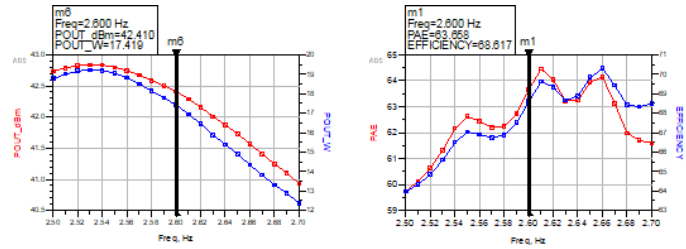


Figure 31: Parallel Amplifier Result

The final EM co-simulation for the fully integrated Parallel Class-E Amplifier was conducted, and the results are shown in Figure 31. There is an adjustment to the total input power (*RF in*) provided to the system. In the single amplifier, the input power used was 28 dBm. However, in this parallel amplifier, the total input power is increased to 31 dBm (approximately 1.26 Watts).

This increase is specifically implemented to compensate for the -3dB power split that occurs at the input hybrid coupler. By providing a total power of 31 dBm at the main input port, the coupler evenly divides this power so that each amplifier branch (Q1 and Q2) is still driven by an input power of approximately 28 dBm. This ensures that each transistor continues to operate at its optimal Class-E operating point, exactly as in the single amplifier design.

With an input power of 31 dBm (1.26 W) at the 2.6 GHz frequency, the parallel amplifier produces an output power (POUT) of 42.410 dBm (17.419 W). The Large Signal Gain at 12.195 dB, while the input return loss (S11) maintains a good matching at -40.365 dB and (S22) at -37.714 dB. The Power Added Efficiency (PAE) achieved is 63.658 %, and the Drain Efficiency (DE) is 68.617 %, with a total DC power consumption of 12.693 W.

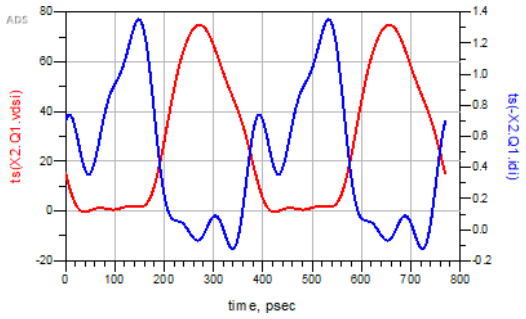


Figure 32: Drain Voltage and Current Waveforms of Power Amplifier 1 (X2).

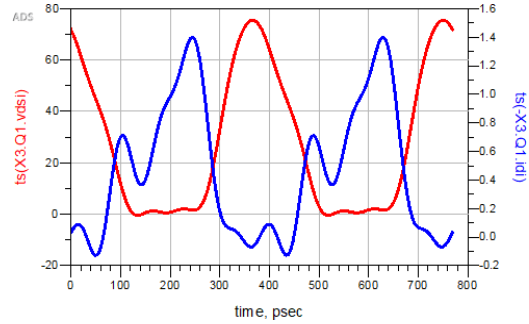


Figure 33: Drain Voltage and Current Waveforms of Power Amplifier 2 (X3).

The graphs above display the time-domain simulation of the drain voltage (red curve) and drain current (blue curve) for the Class-E power amplifier transistors of PA1 (X2) and PA2 (X3). Both graphs prove that the voltage and current curves never overlap simultaneously—when the voltage is at its peak, the current is zero, and vice versa.

J. PCB Implementation and Measurement Setup

The final layout design shown in this study features a fully integrated power amplifier design, while the actual device implementation on the PCB was done using a modular approach, where the hybrid couplers for input and output were made separately and connected via connectors, so that the single amplifier could still be used on its own. But, the final simulation remains the same because, in terms of concept and electrical principles, it's identical to the fabricated result.

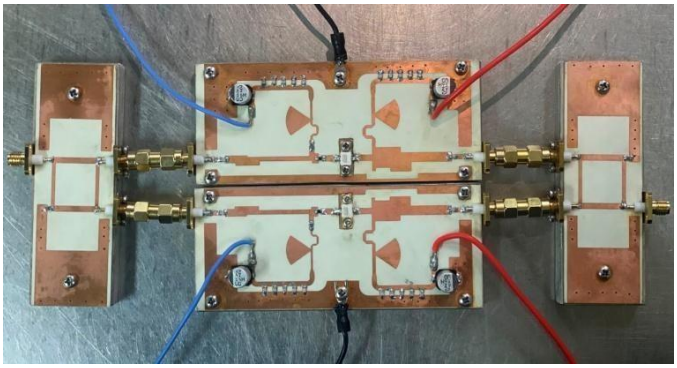


Figure 34: After Fabricated and Implementation of Parallel HPA Class-E with Hybrid Coupler

After fabrication, measurements are made using the Vector Signal Generator (VSG) as the signal source and the Vector Signal Analyzer (VSA) as the analysis of the output signal produced. Figure and Figure 35 below shows the device being tested with VSG, VSA and power supply.

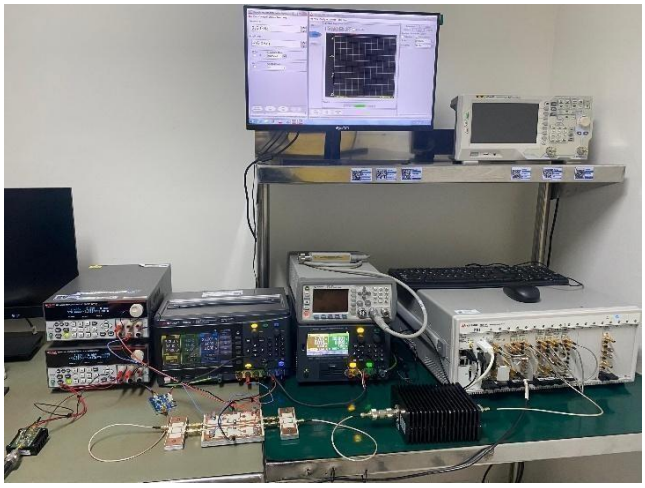


Figure 35: Measurement Parallel HPA Class-E Using VSG, VSA & Power Supply

Tabel 1. Testing Result Single HPA Class-e

P_Output (dBm) Single	P_Output (Watt) Single	Gain (dB) Single	IDC (Ampere) Single	PDC (Watt) Single	PAE (%) Single	Efficiency (%) Single
8	0.063	8	0.016	0.476	1.12	1.33
9	0.079	8	0.018	0.476	1.46	1.67
10	0.01	8	0.025	0.476	1.68	2.1
11	0.00126	8	0.028	0.476	2.23	2.65
12	0.0159	8	0.031	0.504	2.55	3.15
13	0.02	8	0.035	0.504	3.36	3.96
14	0.0251	8	0.04	0.532	3.97	4.72
15	0.0316	8	0.046	0.56	4.75	5.65
16	0.0398	8	0.0515	0.616	5.43	6.46
17	0.0501	8	0.0595	0.672	6.27	7.46
18	0.0631	8	0.0665	0.728	7.29	8.67
19	0.0796	8	0.0745	0.812	8.16	9.78
20	0.1	8	0.084	0.896	9.38	11.16
21	0.1259	8	0.1065	1.008	10.51	12.49
22	0.1585	8	0.1185	1.12	11.92	14.15
23	0.1995	8	0.1335	1.26	13.3	15.84
24	0.2512	8	0.1505	1.4	15.09	17.94
25	0.3981	8	0.1675	1.596	16.68	19.81
26	0.3981	8	0.182	1.764	19	22.57
27	0.5012	8	0.2005	1.988	21.24	25.21
28	0.631	8	0.2186	2.24	23.7	28.17
29	0.7943	8	0.233	2.52	26.52	31.52
30	1.2	8	0.251	2.828	29.77	35.36
31	1.2589	8	0.2745	3.136	33.62	40.14
32	1.5843	8	0.298	3.472	33.77	45.65
32.4	1.7378	7.4	0.31	3.864	33.77	44.97
33	1.9953	7	0.345	4.284	36.8	46.57
33.2	2.0893	6.2	0.364	4.704	37.28	44.42
33.7	2.3442	5.7	0.383	5.096	38.42	46

Tabel 2. Testing Result Parallel HPA Class-e

P_input (dBm)	P_input (Watt)	P_Output (dBm)	P_Output (Watt)	Gain (dB)	IDC_total (Ampere)	PDC_total (Watt)	PAE %	Efficiency (%)
0	0.001	14.3	0.027	14.2	0.032	896	2,892	3,004
1	0.001	15.2	0.033	14.3	0.036	1,008	3,160	3,285
2	0.002	17.6	0.058	15.3	0.05	1,400	3,997	4,110
3	0.002	18.3	0.068	15.4	0.056	1,568	4,185	4,312
4	0.003	19.4	0.087	15.6	0.062	1,736	4,872	5,017
5	0.003	21	0.126	15.9	0.07	1,960	6,262	6,423
6	0.004	21.9	0.155	16	0.08	2,240	6,737	6,914
7	0.005	23.4	0.219	16.3	0.092	2,576	8,298	8,493
8	0.006	24.3	0.269	16.4	0.103	2,884	9,114	9,333
9	0.008	25.5	0.355	16.5	0.119	3,332	10,410	10,649
10	0.01	26.4	0.437	16.6	0.133	3,724	11,453	11,722
11	0.013	27.7	0.589	16.7	0.149	4,172	13,812	14,114
12	0.016	28.5	0.708	16.8	0.168	4,704	14,713	15,050
13	0.02	29.9	0.977	16.9	0.217	6,076	15,755	16,084
14	0.025	30.7	1.175	16.8	0.237	6,636	17,326	17,705
15	0.032	31.7	1.479	16.7	0.267	7,476	19,362	19,785
16	0.04	32.6	1.82	16.6	0.301	8,428	21,119	21,591
17	0.05	33.5	2.239	16.5	0.335	9,380	23,333	23,867
18	0.063	34.1	2.57	16.1	0.364	10,192	24,601	25,220
19	0.079	34.9	3.09	15.9	0.401	11,228	26,815	27,523
20	0.1	35.6	3.631	15.6	0.437	12,236	28,856	29,673
21	0.126	36.1	4.074	15.1	0.466	13,048	30,257	31,222
22	0.158	36.8	4.786	14.8	0.502	14,056	32,924	34,052
23	0.2	37.5	5.623	14.5	0.543	15,372	35,284	36,592
24	0.251	38	6.31	14	0.596	16,688	36,303	37,809
25	0.316	38.4	6.918	13.4	0.64	17,920	36,842	38,607
26	0.398	38.9	7.762	12.9	0.69	19,320	38,118	40,178
27	0.501	39.2	8.318	12.2	0.728	20,384	38,346	40,805
28	0.631	39.6	9.12	11.6	0.766	21,488	39,580	42,552
29	0.794	40.1	10.233	11.1	0.784	21,952	42,996	46,615
30	1	40.7	11.749	10.7	0.83	23,240	46,252	50,555
31	1.259	41.2	13.183	10.2	0.87	24,360	48,948	54,116

Here are the formulas for performance parameters used to process the test result data:

RF Input Power (Watt):

$$P_{in}(W) = 10^{\left(\frac{P_{in}(\text{dBm})-30}{10}\right)}$$

RF Output Power (Watt):

$$P_{out}(W) = 10^{\left(\frac{P_{out}(\text{dBm})-30}{10}\right)}$$

Power Gain (dB):

$$P_{gain}(\text{dB}) = P_{out}(\text{dBm}) - P_{in}(\text{dBm})$$

Drain Efficiency (%):

$$\text{Efficiency } (\%) = \left(\frac{P_{out}(W)}{P_{DC\_total}(W)}\right) \times 100$$

Power Added Efficiency (PAE (%)):

$$\text{PAE } (\%) = \left(\frac{P_{out}(W) - P_{in}(W)}{P_{DC\_total}(W)}\right) \times 100$$

Here's an explanation of the formula for calculating the total current (IDC_total) and total DC power (PDC_total), adjusted for a two-parallel amplifier architectureTotal DC Current (Ampere):

$$I_{DC\_total} = I_{DC1} + I_{DC2}$$

Total DC Power (PDC_total (Watts)):

$$P_{DC\_total}(W) = V_{DS} \times I_{DC\_total}$$

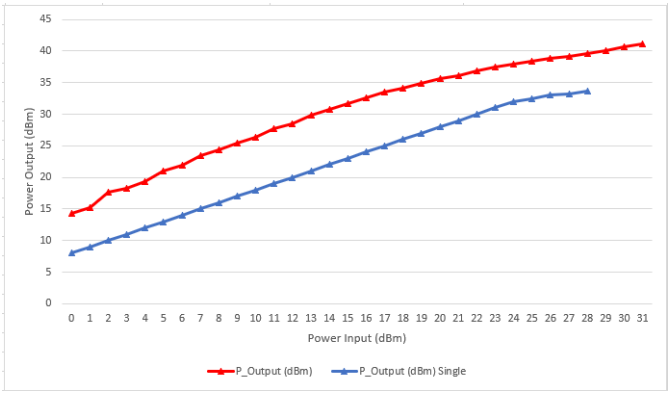


Figure 36: Result Testing of Power Output (dBm) vs Power Input (dBm)

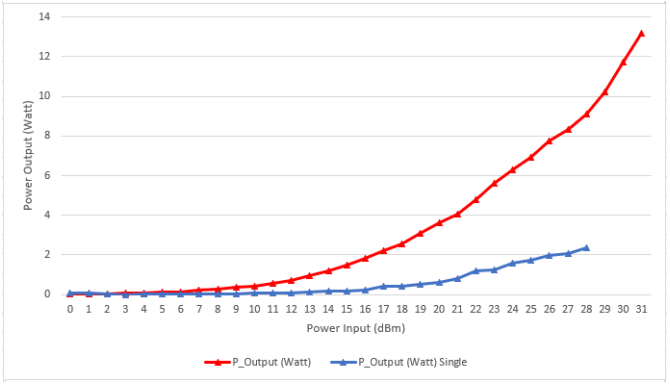


Figure 37: Result Testing of Power Output (Watt) vs Power Input (Watt)

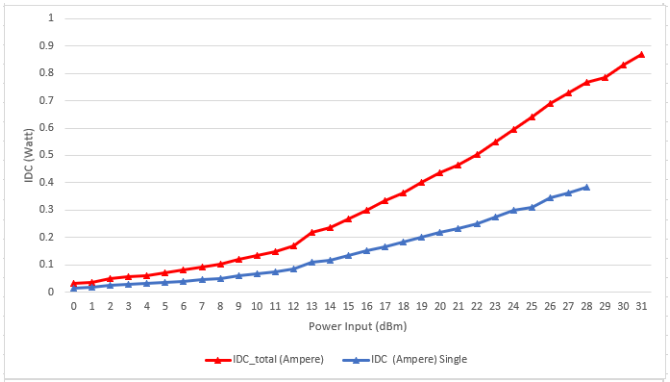


Figure 38: Result Testing of IDC_total (Ampere) vs Power Input (dBm)

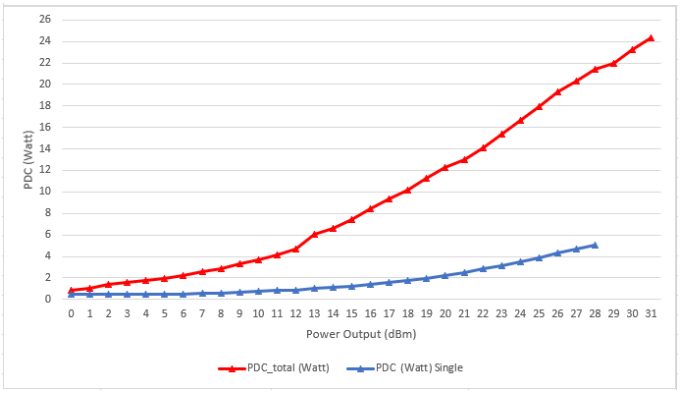


Figure 39: Result Testing of PDC_total (Watt) vs Power Input (dBm)

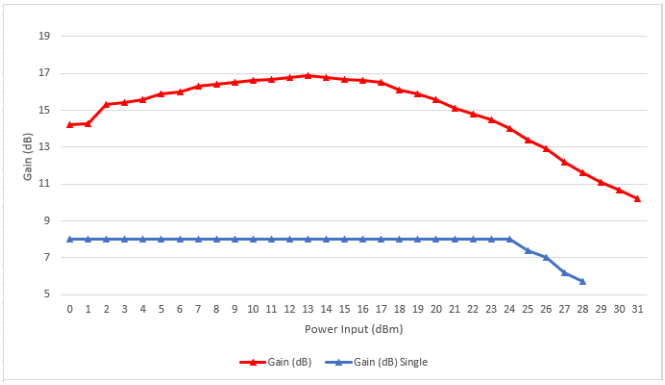


Figure 40: Result Testing of Gain (dB) vs Power Input (dBm)

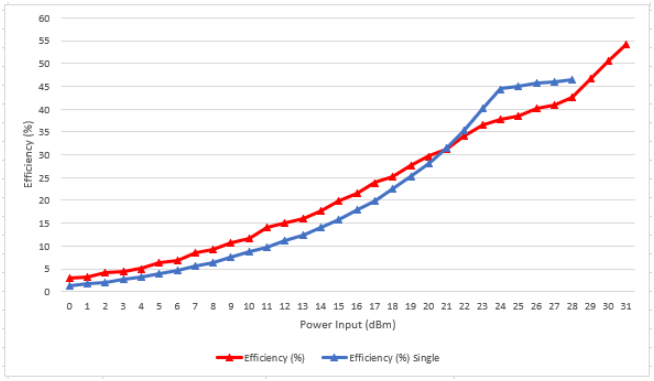


Figure 41: Result Testing of Efficiency (%) vs Power Input (dBm)

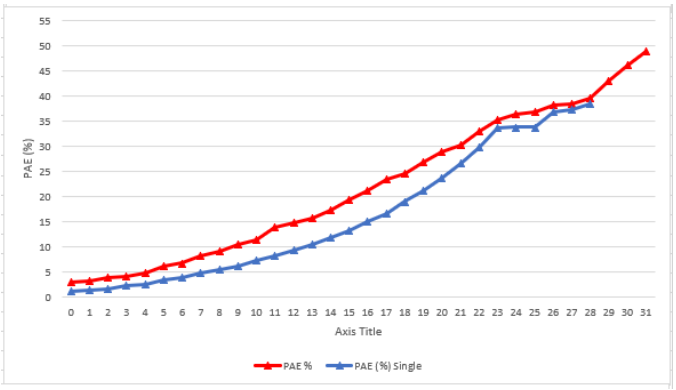


Figure 42: Result Testing of PAE (%) vs Power Input (dBm)

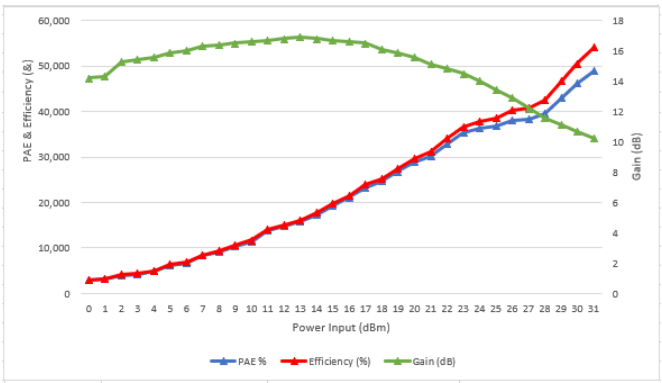


Figure 43: Result Testing Comparing of Gain (dB), PAE (%), and Efficiency (%) vs Power Input (dBm) Parallel.

IV. CONCLUSION

In summary, the design, simulation, PCB fabrication (Figure 34), and experimental testing (Figures 36 to 41) of the high-power and high-efficiency RF Class-E parallel power amplifier integrated with hybrid couplers using GaN HEMT transistors (CGH40010F) have been successfully accomplished for 2.6 GHz wireless power transfer (WPT) applications.

Based on the precise experimental test results from the measurement table validated against the Advanced Design System (ADS) electromagnetic co-simulation, at the maximum input power (P_in) of 31 dBm (1.259 W), the electromagnetic co-simulation yielded an output power of 42.410 dBm (17.419 W), whereas actual experimental testing successfully delivered a measured output power (P_out) of 41.2 dBm (13.183 W) with a power gain of 10.2 dB. At this maximum operating point, the practical measurement recorded a total DC power consumption (P_DC) of 24.360 W (0.87A x 28V), a Power-Added Efficiency (PAE) of 48.948%, and a drain efficiency of 54.116%.

A performance variation is observed between the ideal simulation and practical measurement results at this maximum input level. Specifically, the drain efficiency decreased from 68.617% (simulation) to 54.116% (testing), and the PAE decreased from 63.658% (simulation) to 48.948% (testing), while the total DC power consumption increased from 12.693 W in simulation to 24.360 W during testing. This performance decrease and power consumption increase are primarily attributed to dimensional deviations in microstrip trace widths and lengths during PCB fabrication, etching precision limitations on the Rogers RO4350 substrate (20 mils), solder joint parasitics, and connector insertion losses.

For subsequent fabrications, tighter parameter controls are recommended during PCB manufacturing specifically regarding layer film processing, etching precision, and thermal management mounting to achieve performance results that more closely align with simulations. Nonetheless, the fabricated parallel Class-E amplifier successfully provides a robust high output power of 13.183 W at 31 dBm input, serving as a practical, scalable high-power transmitter solution for advanced wireless power transfer (WPT) systems.

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FORMULIR LOOGBOOK BIMBINGAN DAN PENGAJUAN
SEMINAR PROPOSAL/SIDANG TUGAS AKHIR/ PROYEK AKHIR*

Nama : M. Adha Alhafiz
NIM 3222311035
Pembimbing : Dr. Ir. Basuki Rachmatul Alam
Judul : Design and Implementation of a High-Power and High-Efficiency RF Class-E Parallel Amplifier with Hybrid Coupler Using GaN HEMT Transistors for Wireless Power Transfer.

No	Hari/Tgl	Rincian Kegiatan	TTD Pembimbing
1	Rabu, 11 Februari 2026	Membahas rencana perancangan terkait penelitian kedepan setelah selesai revisi seminar proposal.	
2	Jumat, 13 Februari 2026	Membahas perancangan skematik Class-E HPA dan desain matching network (input/output).	
3	Rabu, 06 mei	Pembahasan terkait perencanaan transistor GaN HEMT yang di pakai.	
4	Rabu, 03 Juni 2026	Mendiskusikan desain dan optimasi 3dB Hybrid Coupler untuk pembagi daya (dividing) dan penggabung (combining).	
5	Senin, 15 Juni 2026	Membahas Simulasi DC IV Characterization GaN HEMT dan penentuan operating point (bias point).	
6	Senin, 22 Juni 2026	Diskusi terkait target capaian dari desain layout PCB Balanced Amplifier.	
7	Rabu, 08 Juli 2026	Revisi untuk mengganti Tansistor dari 300 Watt menjadi 10 Watt dan dibuat persingle Amplifier	
8	Jumat, 10 Juli 2026	Membahas capaian semua tahapan desain yang telah dibuat dan menyiapkan jurnal Proyek Akhir	
9	Kamis, 22 Juli 2026	Membahas revisi erkait jurnal Proyek Akhir yang sudah dibuat	
10			

Berdasarkan hasil bimbingan yang telah dilaksanakan selama 3 bulan dan telah disetujui oleh dosen pembimbing, maka dengan ini saya mengajukan diri sebagai peserta Sidang Tugas Akhir/ Proyek Akhir.

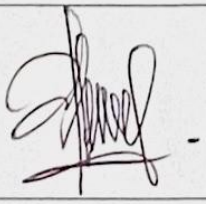
Batam, 22 Juli 2026
Peserta

M. Adha Alhafiz

**Hapus yang tidak perlu.*
Jumlah bimbingan minimal 10 kali. Dalam satu minggu maksimal bimbingan yang dihitung adalah 2 kali.

Job Assignment Matrix

Company Name : TFME (Teaching Factory Manufacturing of Electronics) Politeknik Negeri Batam.
Department : Radio Frequency Laboratory.
Effective Date : 15 September 2025 – 14 September 2026.

No.	Employee Name	Department	Job Title	Assigned Work / Responsibility
1.	Dr. Ir. Basuki Rachmatul Alam	Manufacturing Electronic Engineering (RF Semiconductor)	Lecturer & Mentor	
2.	M. Adha Alhafiz	Radio Frequency Laboratory	Design & Manufacturing Procces RF	

Prepared By	Approved By
Name: M. Adha Alhafiz **Position:** Internship Student **Date:** 13 Agustus 2026	**Name:** Dr. Ir. Basuki Rachmatul Alam **Position:** Lecturer & Mentor **Date:** 13 Agustus 2026

BERITA ACARA PENYERAHAN HASIL PROYEK
Nomor: -
Tanggal ... Agustus 2026

PELAKSANAAN KEGIATAN
MAGANG DAN PROYEK AKHIR

Pada hari ini Kamis tanggal 13 Agustus 2026, yang bertandatangan di bawah ini:

1. Nama : M. Adha Alhafiz
   Jabatan : Mahasiswa Magang
   Alamat : Perumahan Bunga Raya, Blok M, No. 12, Belian, Batam Kota

Selanjutnya dalam hal ini disebut **PIHAK KESATU**

2. Nama : Dr. Ir. Basuki Rachmatul Alam
   Jabatan : Dosen dan Mentor Magang
   Alamat : Politeknik Negeri Batam

Selanjutnya disebut sebagai **PIHAK KEDUA**

Pihak kedua menerima dari Pihak Pertama berupa :

- ☑ Laporan proyek akhir
- ☑ Laporan magang
- ☑ Hasil proyek:
  - ☑ Produk
  - ☐ Layanan
  - ☐ Prosedur
- ☐ .....

Demikian Berita Acara ini dibuat dan ditandatangani dalam rangkap 2 (dua) untuk dipergunakan sebagai mestinya.

Pihak Kesatu	Pihak Kedua
Mahasiswa Magang	**Mentor Magang**
M. Adha Alhafiz	**Dr. Ir. Basuki Rachmatul Alam**
NIM. 3222311035	NIK. 122274